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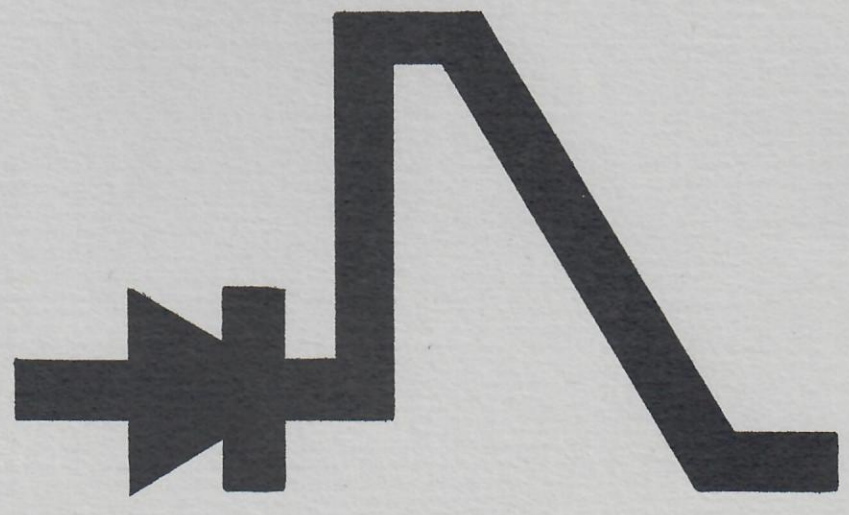
ANSWER MANUAL

PULSES & WAVESHAPING BOOK V



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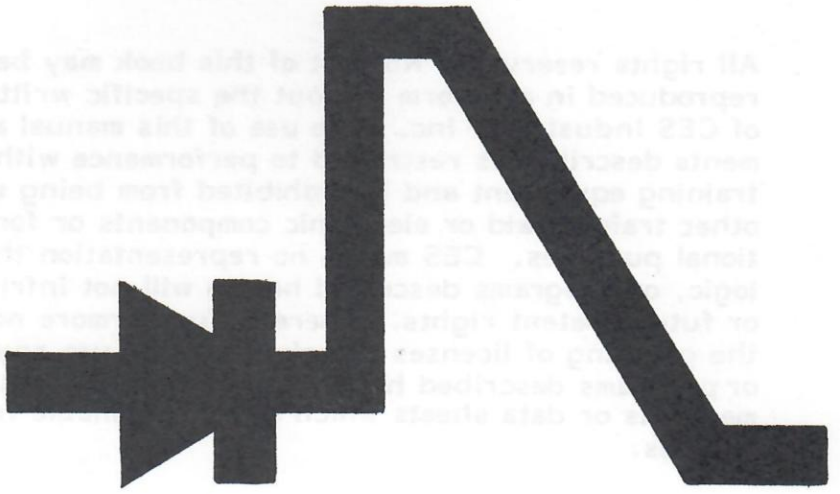

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PULSES & WAVESHAPING BOOK V

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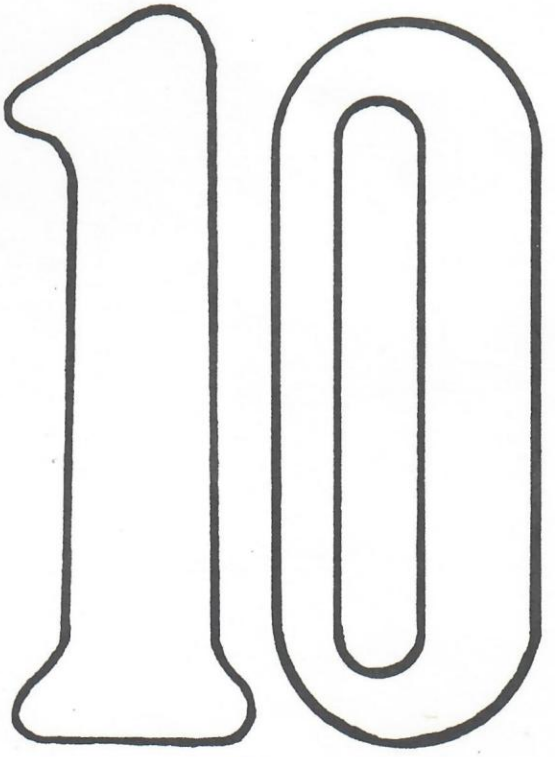

UNIT NO.

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TRANSISTOR SWITCH OR INVERTER

This experiment introduces the transistor used as a solid-state switching device where it is not biased in the linear operating region but is either full ON or full OFF. This is the basic principle of operation of the Digital Logic Inverter or NOT gate.

2.

INPUT SWITCH A	COLLECTOR OUTPUT VOLTAGE
UP	0.2 volts
DOWN	9.5 volts

3. The meter pulses are synchronized with the operation of the switch.

5. ACTUAL OUTPUT "ZERO" VOLTS = 0.05 volts

EXERCISES:

1.

ZERO VOLTS OUTPUT (SILICON) = 0.07 v

BISTABLE MULTIVIBRATOR

Two of the "pulse inverter" circuits from Unit 10 Experiment No. 1 are connected so that the collector output of each drives the base input of the other. This circuit is a BISTABLE MULTIVIBRATOR which is used as a binary memory circuit. Another application of this circuit is to sense very short pulses since a short pulse may be used to "switch" the Bistable Multivibrator to the opposite state.

2.

SET FLIP-FLOP	READ OUTPUT
Momentary Ground	Voutput Collector
C4	8.4 volts
C5	0
C4	8.4 volts
C5	0
B4	0
B5	8.4 volts
B4	0
B5	8.4 volts

QUESTIONS

1. What is the output voltage on collector C4 when the voltage on C5 is zero volts?

   When the collector of C5 is Zero Volts the base voltage on Q4 must be zero. Therefore, Q4 must be off and the collector voltage of Q4 measured at C4 will be 8.4 volts or "high" voltage.

CAPACITOR PULSER

The Pulser or One Shot circuit is investigated. Note that the component values selected will cause the pulse generated to be long enough to observe using the meter. It is not necessary to use an oscilloscope to measure the pulse. Do not operate the switch too quickly, you must give the R-C network time to discharge to see the falling edge of the output pulse.

In order to calculate the time duration of the output pulse we must solve the equation given in the experiment.

$$2\,e^{-\Delta T/RC} = 1$$

The algebra for the solution is:

$$\ln(2e^{-\Delta T/RC}) = \ln(1)$$

$$\ln(2) + \ln(e^{-\Delta T/RC}) = \ln(1) = 0 \qquad \text{Note } \ln(1) = 0$$

$$\ln 2 - \Delta T/RC(\ln e) = 0$$

$$\ln 2 - \Delta T/RC = 0 \qquad \text{Note: } \ln(e) = 1$$

$$\frac{\Delta T}{RC} = \ln 2 = 0.69$$

$$\Delta T = (0.69)(RC)$$

if R = 33K

and C = 100 mfd

$$\Delta T = 0.69(33\times10^{3})(100 \times 10^{-6}) = (69)(33) \times 10^{-3}$$

$$\Delta T = 2.2 \text{ seconds}$$

2.

INPUT: SWITCH A	OUTPUT: PULSE-WIDTH
UP THEN DOWN	3 seconds

CAPACITOR PULSER

3.

Input Switch A: UP then DOWN

R_b	C	Measure PULSE WIDTH
100K	100 mfd	9 Seconds
56K	100 mfd	5 Seconds
56K	10 mfd	1 Second
100K	10 mfd	1.5 Seconds
56K	20 mfd	1.5 Seconds

QUESTIONS:

1. What would the "pulse-width" be for R = 10K and C = 0.001 mfd?

Using the formula derived in this answer manual

$$\Delta T = 0.69\ RC = 0.69(10 \times 10^{3})(0.001 \times 10^{-6})$$

$$\Delta T = 0.69(0.001) \times 10^{-2} = 0.69 \times 10^{-5} = 6.9 \times 10^{-6}$$

$$\boxed{\Delta T = 6.9 \text{ microseconds}}$$

ASTABLE MULTIVIBRATOR

This experiment tests the Astable Multivibrator circuit. The Astable Multivibrator is used as an inexpensive and easy to build square wave generator which is suitable for use as a clock for digital circuits. Since the frequency depends on the RC time constant the stability and frequency accuracy is not outstanding and the circuit maximum frequency is generally limited to less than 200 KHz but the convenience and reliability make it popular for general usage. Also it is useful for low frequency generation.

2.

OUTPUT 0 - 9.2 volts, 8 Seconds Period

4.

POSITIVE VOLTAGE TIME = 2 Seconds
ZERO VOLTAGE TIME = 4 Seconds

5.

PERIOD = 6 seconds

6.

$$\text{DUTY CYCLE} = \frac{\text{PULSE WIDTH}}{\text{TOTAL PERIOD}} \times 100\% = 33\%$$

R 1 = R 2 = 33K Duty Cycle = 50%

R 1 = 56K R 2 = 22K Duty Cycle = 33%

7.

(R 1 = R 2 = 33K) FREQUENCY = 0.12 Hz = 7.5 cycle/min

(R 1 = 56K, R 2 = 22K) FREQUENCY = 0.16 Hz = 10 cycle/min

MONOSTABLE MULTIVIBRATOR

A more sophisticated pulser or Monostable Multivibrator is built using feedback from the pulse output to make the input more sensitive and to make the turn ON and turn OFF points in the pulser much sharper.

3.

OUTPUT PULSE	
OFF LEVEL	0 VOLTS
ON LEVEL (PULSE)	6.4 VOLTS
ON TIME	3 SECONDS

Note that transistor Q5 must have enough gain (high enough Beta) to turn completely ON with the 33K base resistor. If the base resistor is increased a value will be reached where the Monstable Multivibrator will not stay LOW between triggers.

EMITTER COUPLED MULTIVIBRATORS

This is an example of the classification of Emitter coupled transistor circuits where the necessary feedback is generated by the emitter voltage generated across an emitter resistor which is common to both transistors. Note that the positive emitter voltage generated across the emitter resistor makes it possible to turn the NPN transistors OFF at positive values of base voltage. As long as the base voltage is less than the emitter voltage the transistor will be OFF.

2.

Voltage at B = 3.5 volts

3.

PLUS lead from +V2 (Momentarily connect to)	OUTPUT VOLTAGE (Switch A UP)
SET (B) (Base Q4)	9.6 volts
CLEAR (A) (Base Q5)	5.2 volts

4.

GROUND lead (Momentarily connect to)	OUTPUT VOLTAGE (Switch A UP)
SET (C) (Collector Q4)	9.6 volts
CLEAR (B) (Base Q4)	5.2 volts

EMITTER COUPLED MULTIVIBRATORS

7.

TRIGGER	OUTPUT VOLTS (Switch A UP)
PLUS Lead to (B) (Base Q4)	VOLTS (LOW) = 5.2 volts VOLTS (HIGH) = 9.6 volts TIME = 3 seconds
GROUND Lead to (C) (Collector Q4)	VOLTS (LOW) = 5.2 volts VOLTS (HIGH) = 9.6 volts TIME = 3 seconds

8.

Free-Running Multivibrator	
ON TIME	1 seconds
ON VOLTAGE	9.6 volts
OFF TIME	4 seconds
OFF VOLTAGE	5.2 volts

NOTE: The adjustment of the 100K POT for Astable operation may be difficult. Care must be taken to find the correct voltage for this mode of operation.

COMPLEMENTARY MULTIVIBRATOR

This application illustrates the type of circuit which uses complementary transistors to advantage. The collector current of Q2 the PNP transistor supplies base current to the NPN transistor Q4. This is only possible when using Complementary Transistors.

3.

SET	OUTPUT VOLTS
PLUS TO D	(C) = 9 volts
or	(A) = 3 volts
GROUND TO B	(B) = 0 volts

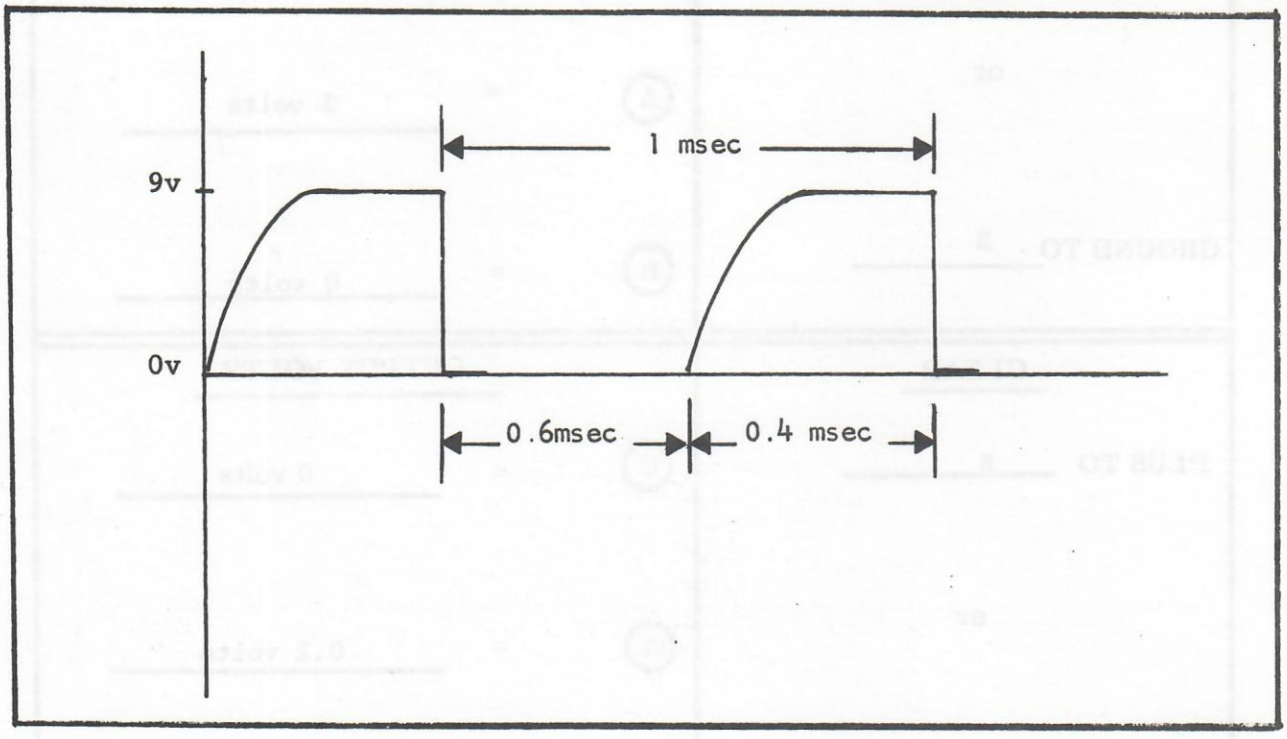
CLEAR	OUTPUT VOLTS
PLUS TO B	(C) = 0 volts
or	(A) = 0.2 volts
GROUND TO C	(B) = 0.2 volts

VARIABLE FREQUENCY PULSE GENERATOR

This Variable Frequency Pulse Generator employs the same circuit used in the Astable Multivibrator, Unit 10 Experiment No. 4. The timing capacitors and resistors are much smaller to provide oscillation at a higher frequency and potentiometers are used in series with the charging base resistors to provide variable frequency and duty cycle at the output.

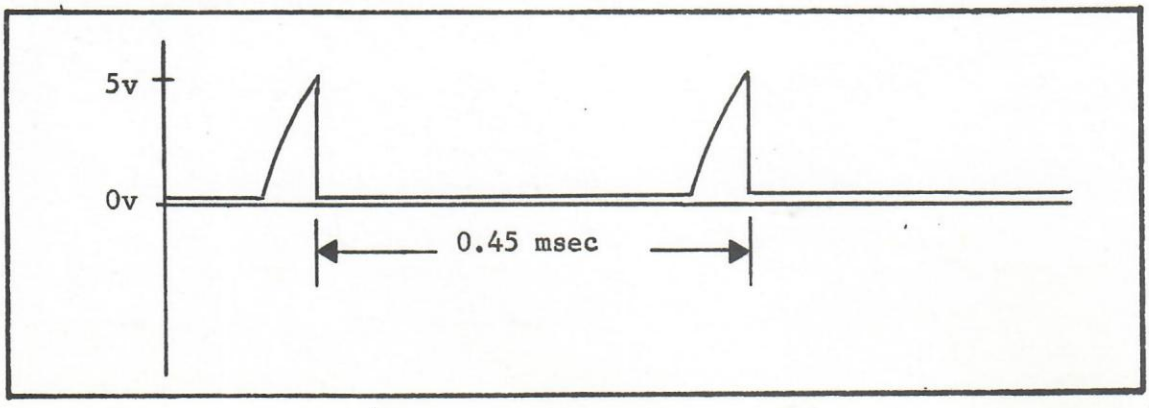
2.

PERIOD = 1 msec



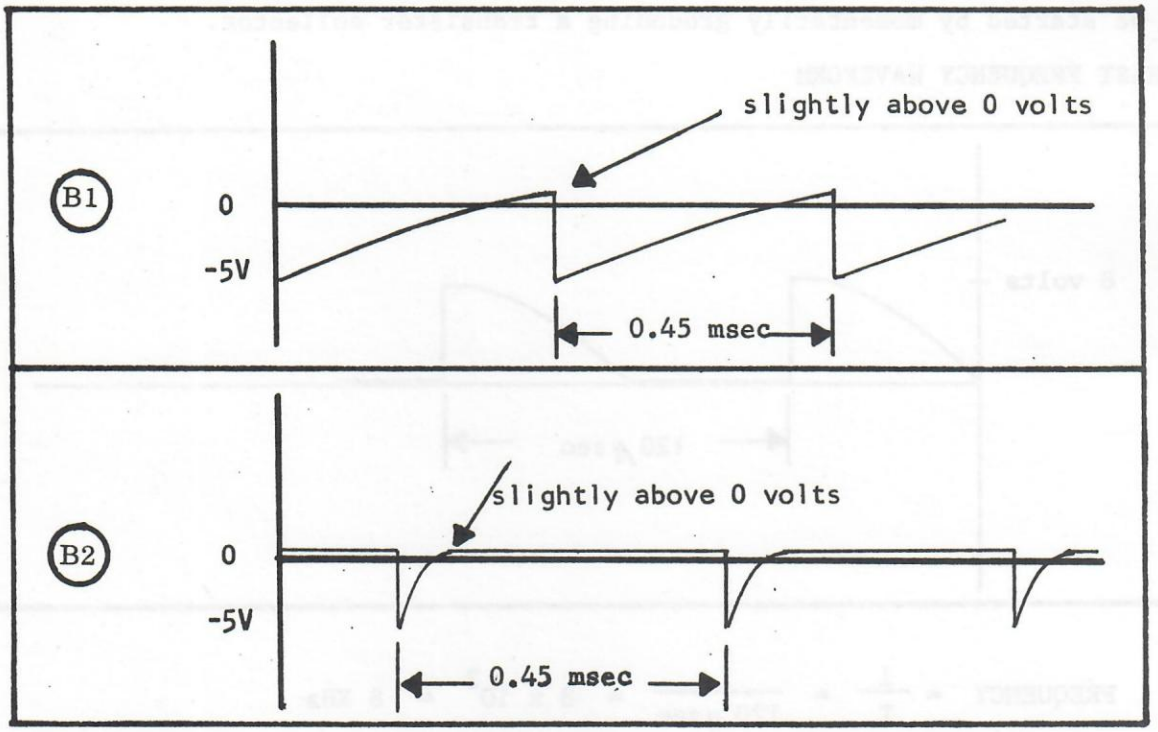
3. The actual measured period was 0.001 seconds so the practical circuit had ½ the period predicted by this formula.

4.



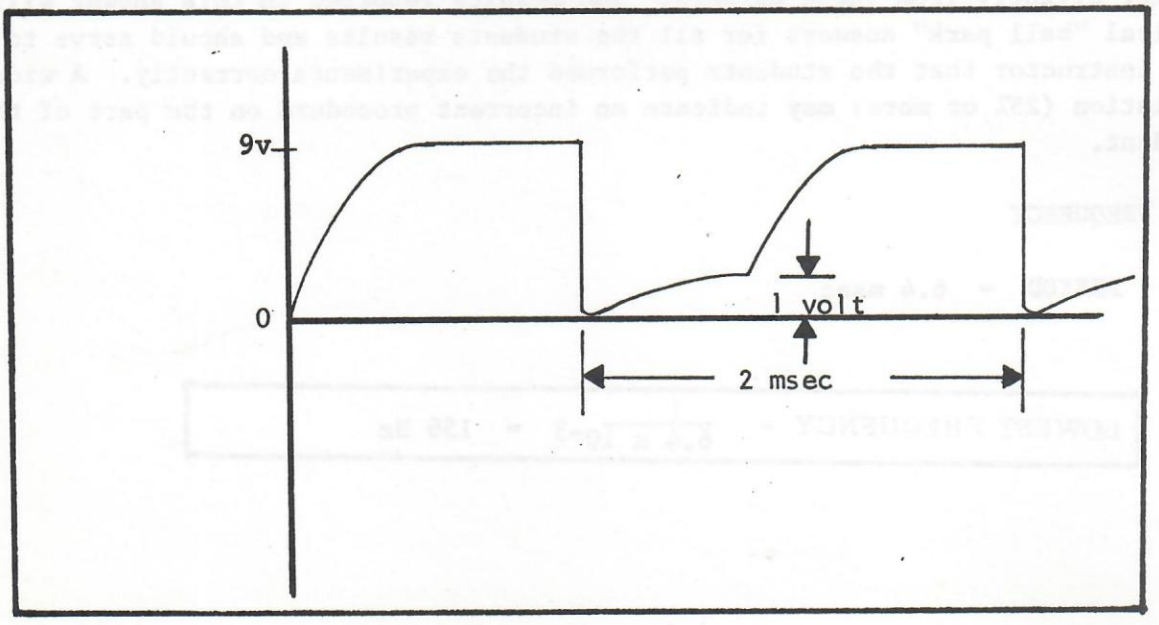
VARIABLE FREQUENCY PULSE GENERATOR

WAVEFORM AT B1 (Base of Q5)



5.

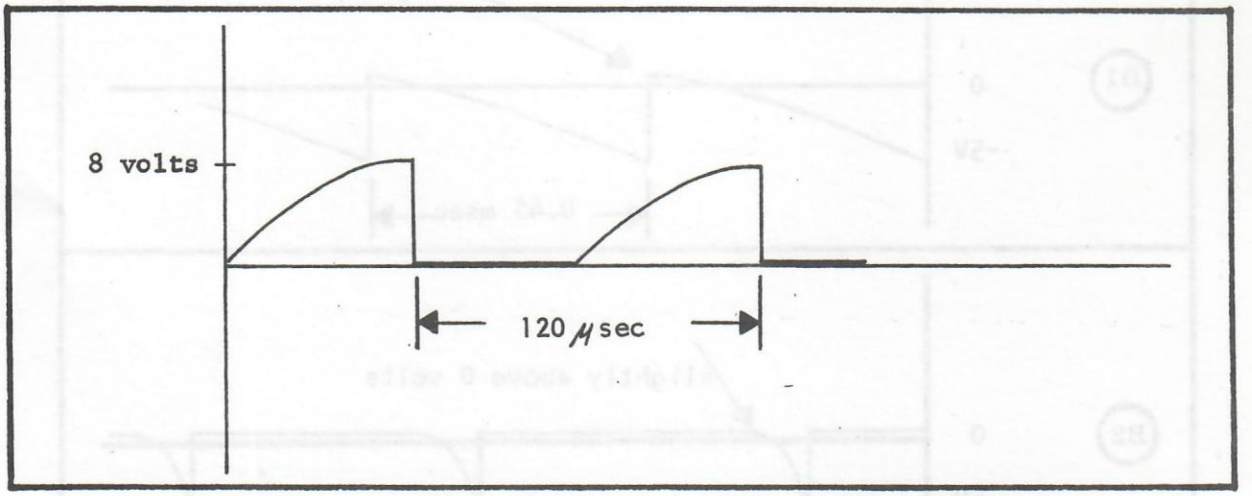
UNSATURATED SIGNAL



VARIABLE FREQUENCY PULSE GENERATOR

6. Note: The oscillator may not start, even when the collectors are momentarily grounded. If this occurs then increase the 100K POT from zero until the oscillator can be started by momentarily grounding a transistor collector.

8. HIGHEST FREQUENCY WAVEFORM



$$\text{FREQUENCY} = \frac{1}{T} = \frac{1}{120\ \mu\text{sec}} = 8 \times 10^{3} = 8\ \text{KHz}$$

Maximum FREQUENCY = 8 KHz

Note: The Maximum and Minimum frequencies will vary from report to report and may differ slightly from these answers. The results reported in this answer will be typical "ball park" answers for all the students results and should serve to assure the instructor that the students performed the experiments correctly. A wide variation (25% or more) may indicate an incorrect procedure on the part of the student.

9. LOW FREQUENCY

PERIOD = 6.4 msec

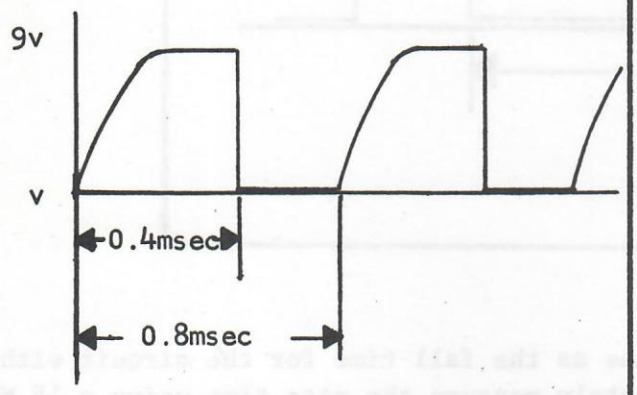
$$\text{LOWEST FREQUENCY} = \frac{1}{6.4 \times 10\text{-}3} = 156\ \text{Hz}$$

VARIABLE DUTY CYCLE AND RISE TIME

The pulse duration of each transistor of an Astable Multivibrator is dependent on the resistance of the base charging resistor. In this circuit the 100K POT is used to unbalance these base resistors. This allows the duty cycle of the pulse generator to be adjusted.

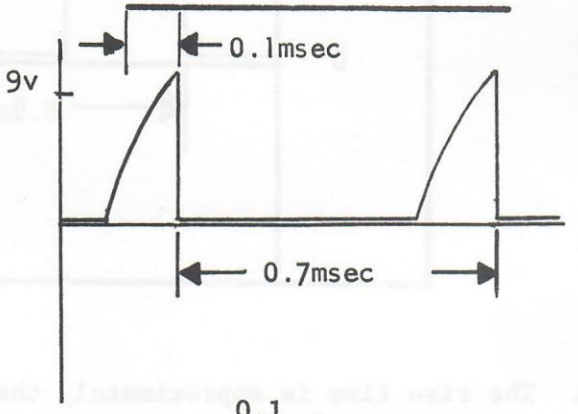
2.

A. EQUAL SPACING



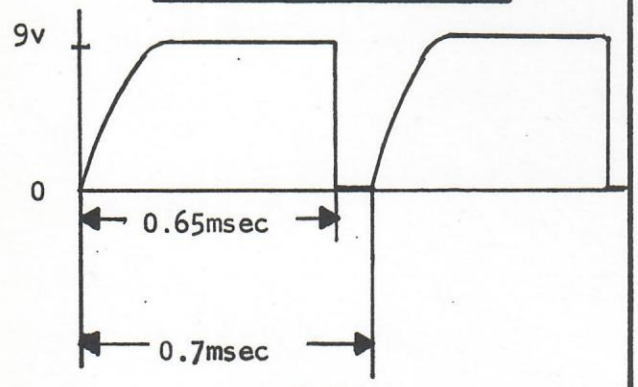
Duty Cycle = 50%

B. SHORTEST PULSE



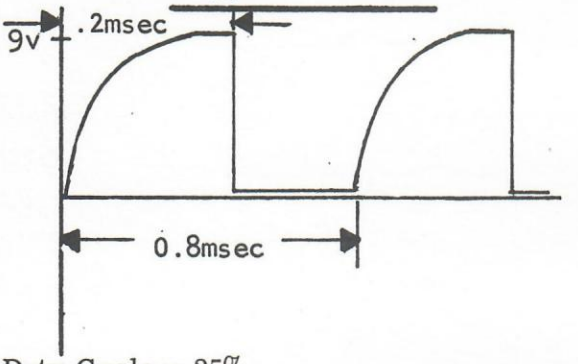
Duty Cycle = $\frac{0.1}{0.7}$ x 100 = 14%

C. WIDEST PULSE



Duty Cycle = $\frac{0.65}{0.70}$ x 100 = 92.8%

D. PULSE



Duty Cycle = 25%

Rise Time = 60 Msec

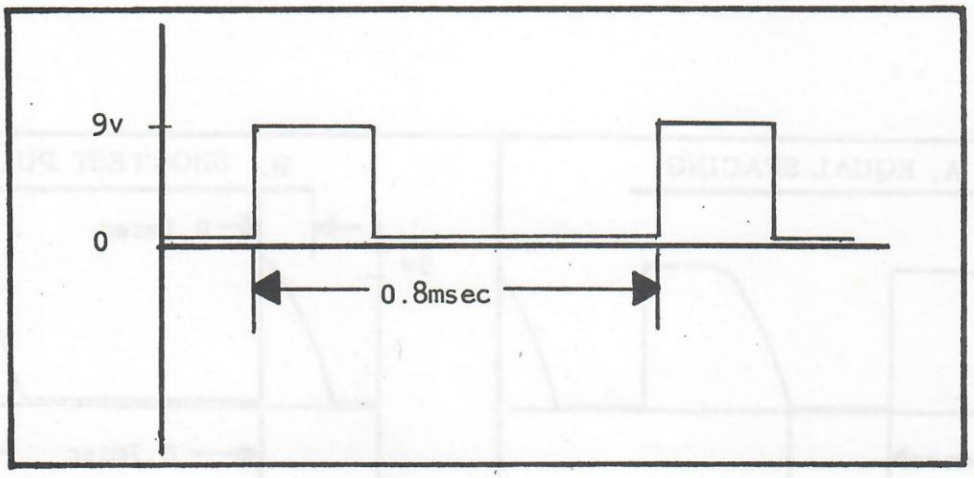
Fall Time = very small

3.

PULSE RISE TIME	= 60 Microseconds
PULSE FALL TIME	= To short to measure

VARIABLE DUTY CYCLE AND RISE TIME

5. Output Waveform

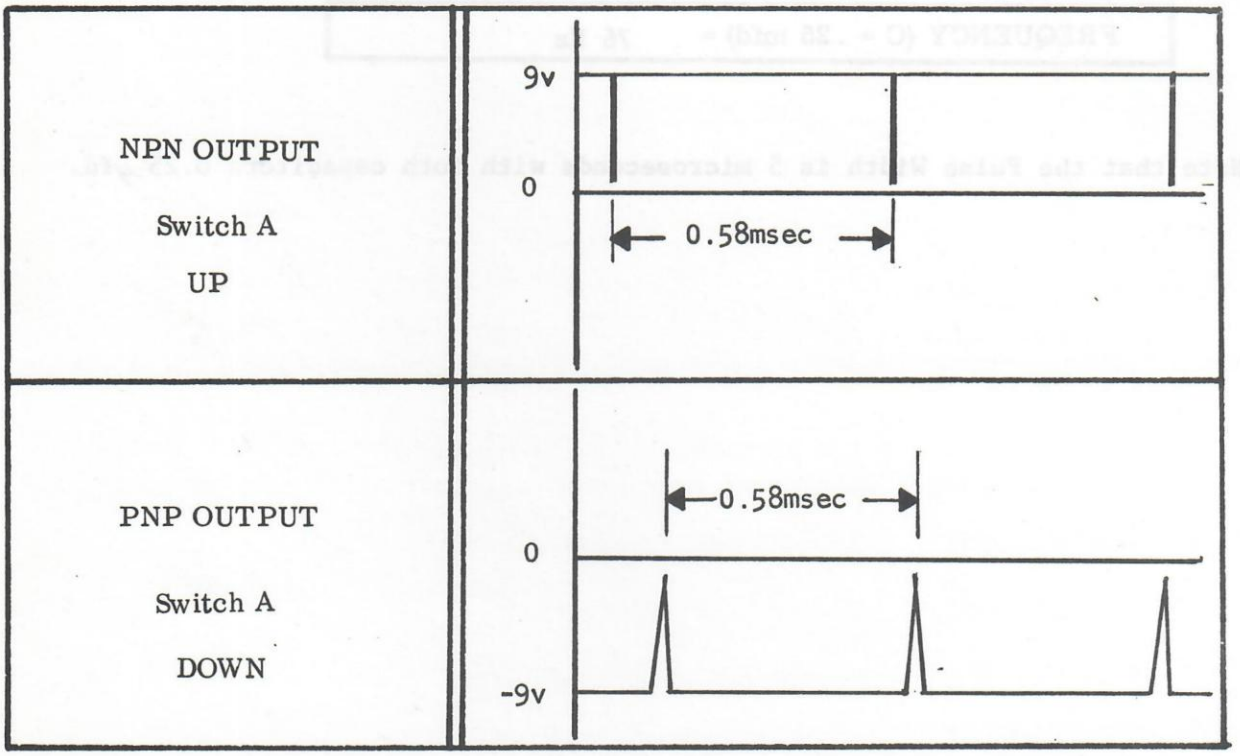


6. The rise time is approximately the same as the fall time for the circuit with the decoupling diode. We could not accurately measure the rise time using a 15 MHz oscilloscope. The rise time must be reported as less that 1 microsecond.

COMPLEMENTARY ASTABLE

This complementary Astable Multivibrator uses a PNP and an NPN transistor. Note that the PNP side uses a negative power supply while the NPN side uses a positive power supply. Note that in this Multivibrator both transistors are either both ON or both OFF.

2.



3.

PERIOD = 0.58 m sec

4. The Period is 58% of the time constant

5.

$$\text{FREQUENCY} = \frac{1}{0.58 \text{ msec}} = 1724 \text{ Hz}$$

6.

PULSE WIDTH = 1.25 microseconds

7. The capacitor connected to the base of Q5 was changed to 0.25μfd. The Pulse Width became much wider (0.1 msec) and the Period change to 0.85 msec.

8. The capacitor to the base of Q1 was changed to 0.25μfd. The Pulse Width became a little wider (0.04 msec) and the period change to 0.65 msec.

COMPLEMENTARY ASTABLE

9. With both capacitors 0.25 μfd;

PERIOD (C = 0.25 mfd)	=	13 msec

FREQUENCY (C = .25 mfd)	=	76 Hz

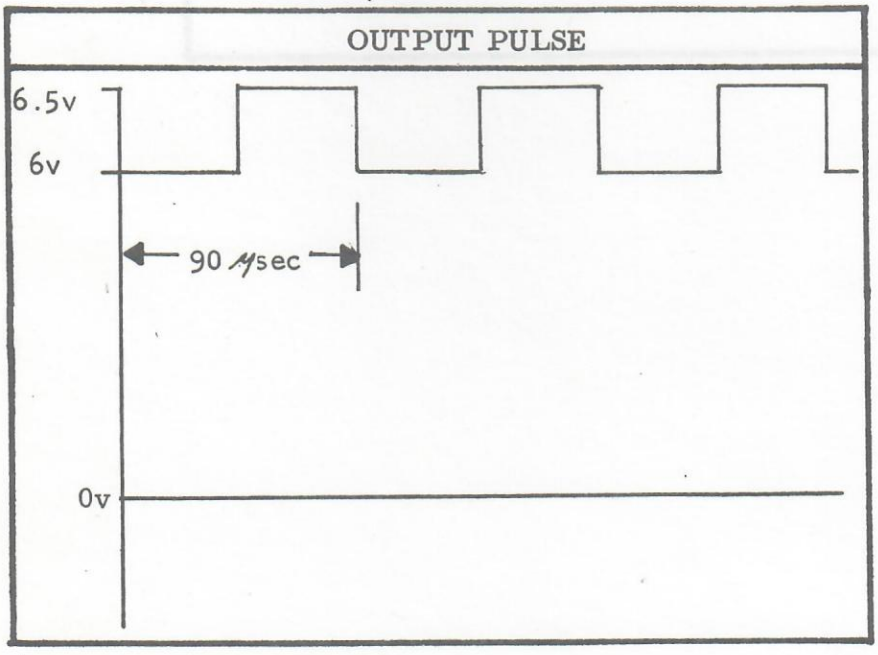
Note that the Pulse Width is 5 microseconds with both capacitors 0.25 μfd.

EMITTER COUPLED ASTABLE

In this ASTABLE MULTIVIBRATOR the transistors are not always cut off or saturated. Note that Q4 is biased in the Active or Linear Region of operation by the 1K resistor connected between the collector and base and by the bias voltage generated at the wiper of the 1K POT. Both transistors cannot be ON at the same time because the emitter of Q5 would then be more positive than the base and the transistor would turn OFF. Both transistors cannot be OFF because Q4 is biased in the active region and Q5 would turn ON due to base current generated from the collector of Q4.

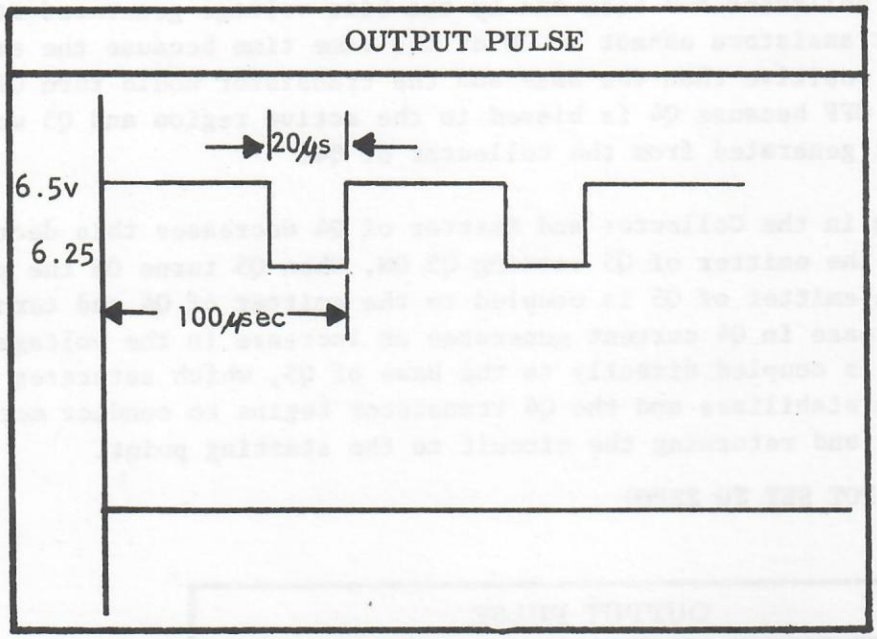
As the current flowing in the Collector and Emitter of Q4 decreases this decreasing voltage is coupled to the emitter of Q5 turning Q5 ON. When Q5 turns ON the positive pulse generated on the emitter of Q5 is coupled to the emitter of Q4 and turns Q4 further OFF. The decrease in Q4 current generates an increase in the voltage on the collector of Q4 which is coupled directly to the base of Q5, which saturates Q5. The capacitor voltage then stabilizes and the Q4 transistor begins to conduct more, decreasing the voltage on Q5 base and returning the circuit to the starting point.

3. OUTPUT PULSE (10K POT SET TO ZERO)



EMITTER COUPLED ASTABLE

4. OUTPUT PULSE (Full 10K)



VARIABLE MONOSTABLE MULTIVIBRATOR

This type of variable pulse Monostable Multivibrator has many applications in digital and pulse circuitry where a variable delay must be generated or where the ON or OFF time of a particular circuit under control must be varied and must be turned ON by a trigger pulse.

3.

PULSE WIDTH (R = 10K) = 2 microseconds

The actual pulse width is shorter than the predicted approximate value but it is of the same order of magnitude.

4.

PULSE WIDTH (maximum) = 93 microseconds

DUTY CYCLE (maximum) = $\frac{93 \text{ sec}}{100 \text{ sec}}$ = 93%

5.

LOADING	EFFECT
A 1K TO GROUND	WIDTH STOPS THE PULSE AMPLITUDE _____
B 1K to GROUND	WIDTH 0.25 microseconds AMPLITUDE 5 volts

VARIABLE MONSTABLE MULTIVIBRATOR

PARAMETER VARIATION 10K Across (Leads Y & Z)	EFFECT ON Pulse Amplitude & Pulse Width
2.2K Collector Resistor	NO EFFECT
3.3K Collector Resistor	NO EFFECT
22K Coupling Resistor	PULSE AMPLITUDE LOWERS FROM 9 VOLTS TO 7 VOLTS
33K Bias Resistor	NO EFFECT
10K Timing Resistor	PULSE WIDTH CHANGES FROM 2 μsec to 0.5 μsec
15K Differentiator Resistor	NO EFFECT

6. The maximum pulse width achieveable without the diode D1 is 50 microseconds. The Duty Cycle is 50%.

TRANSISTOR SWITCH BIASING

This is an example of practical transistor switch which takes into account the fact that the driving or input signal may not actually go to ground. The negative bias assures that when the input voltage drops below a minimum level the switching transistor will turn OFF.

2.

INPUT	INPUT VOLTAGE SWITCH C DOWN
Switch A UP (zero offset)	1.0 volts
Switch A DOWN	8.5 volts

3.

	INPUT	(A) OUTPUT With R_B 100K	(B) OUTPUT Without R_B	(C) OUTPUT Silicon Q7 Without R_B	(D) OUTPUT Silicon Q7 With R_B
Switch A UP zero offset	1.0 volts	8.5 volts	3 volts	6 volts	8.5 volts
Switch A DOWN	8.5 volts	0 volts	0 volts	0 volts	0 volts

4. The circuit output does not go to the full Power Supply voltage of 8.5 volts, indicating that the transistor does not turn OFF.

5. The output when the transistor is OFF is 6 volts. This indicates that the transistor is not fully OFF but that the larger base-emitter voltage of the Silicon Transistor allows less collector current to flow when the base is at the 1 volt positive offset.

TRANSISTOR SWITCHING BIASING

6. The circuit works properly with the 100K R_B connected to -V2. The 8.5 volt output indicates that the Silicon Transistor is fully OFF when the input switch is UP.

7. Negative to Positive Inversion Circuit Figure 13-2.

When the input switch A is DOWN the transistor is turned ON by the base current flowing from +V1 through the 100K resistor. When the input switch is UP the -V1 voltage connected to the transistor base through the 22K resistor turns the transistor OFF. Note that a Negative input voltage will control a Positive output voltage.

Positive to Negative Inversion Circuit Figure 13-3.

When the input switch A is DOWN the transistor is turned ON by the -V1 connected to the 100K base resistor. When the transistor is ON the output voltage is zero. When the input switch A is UP the +V1 voltage drives the base positive and turns the transistor OFF. When the transistor is OFF the output voltage is -V1.

9.

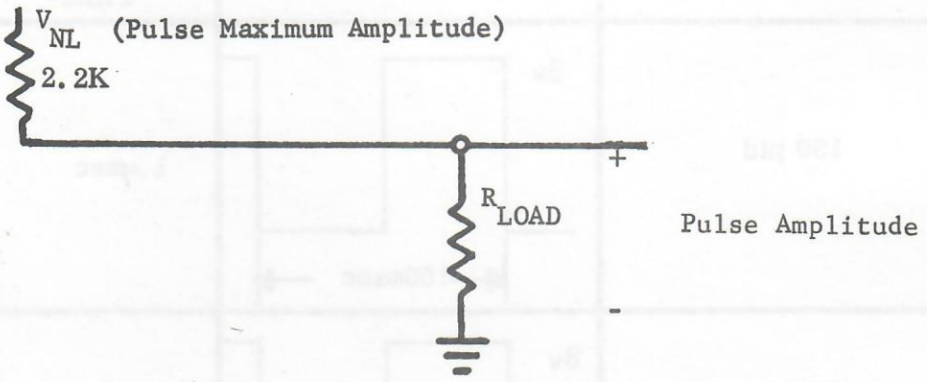
INPUT VOLTS	OUTPUT VOLTS
Switch A UP NEGATIVE	+ 9.0 volts
Switch A DOWN ZERO	+ 0 volts

11.

INPUT VOLTS	OUTPUT VOLTS (negative)
Switch A UP , POSITIVE	— 9.0 volts
Switch A DOWN ZERO	— 0 volts

PULSE CIRCUIT LOADING

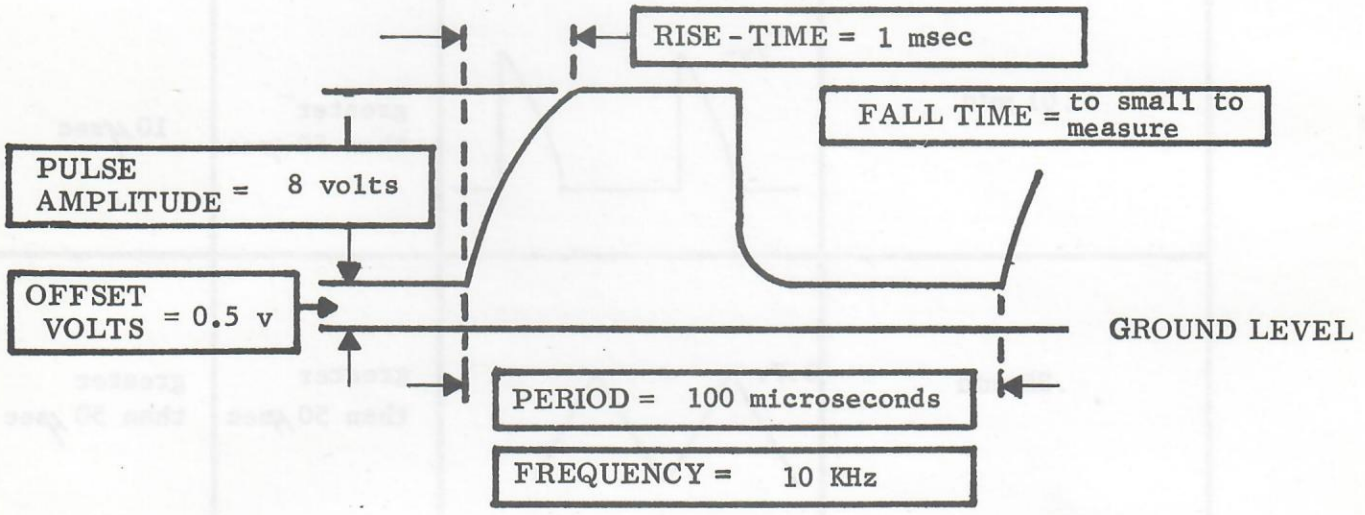
In calculating the Pulse Amplitude for a particular load resistor we can use Ohm's Law and the Voltage Divider Equation to determine the Output Pulse Amplitude.



When the Pulse is at a Positive Value we can apply the Voltage Divider Equation to determine the Pulse Amplitude.

$$\text{Pulse Amplitude} = \frac{V_{NL}\ R_{LOAD}}{R_{LOAD} + 2.2K}$$

3.


RISE-TIME = 1 msec
FALL TIME = to small to measure
PULSE AMPLITUDE = 8 volts
OFFSET VOLTS = 0.5 v
GROUND LEVEL
PERIOD = 100 microseconds
FREQUENCY = 10 KHz

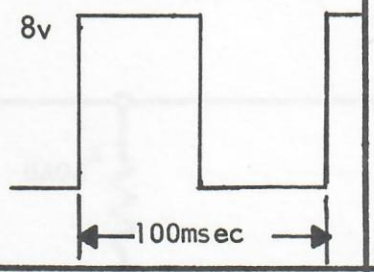
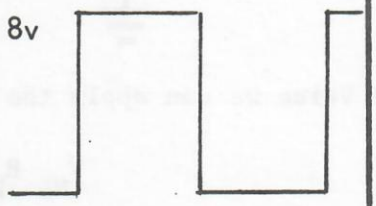
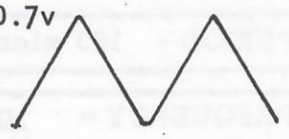
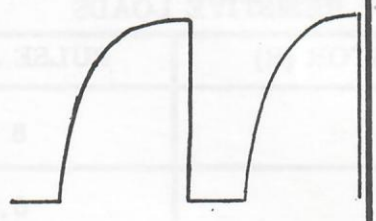
4.

RESISTIVE LOADS

LOAD RESISTOR (R)	PULSE AMPLITUDE
100K	8 volts
10K	6.5 volts
2.2K	4 volts
1K	2 volts
100 ohms	0.2 volts

PULSE CIRCUIT LOADING

5. CAPACITIVE LOADS

Capacitance	Waveform	Rise Time	Fall Time
150 pfd		1 μsec	less than 0.1 μsec
.001 mfd		2 μsec	less than 0.1 μsec
.01 mfd		greater than 50 μsec	10 μsec
.25 mfd		greater than 50 μsec	greater than 50 μsec
(Capacitance between your two hands.)		10 μsec	50 μsec

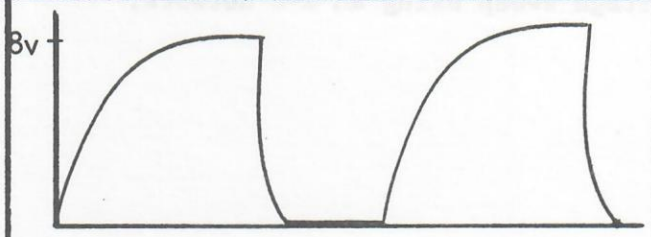
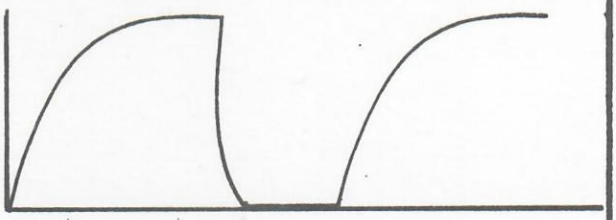
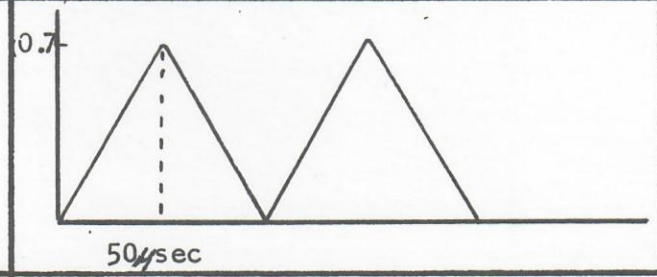
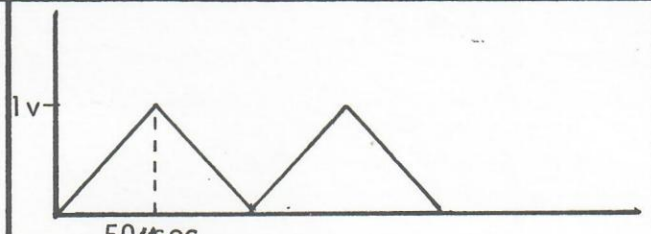
The resistance between the hands is large compared to 2.2K because the pulse reaches the full 8 volt unloaded output level. The rise time indicates that the capacitance is between 0.01 and 0.001 mfd, or perhaps 0.005 mfd.

LOW PASS R.C. CIRCUIT

When a pulse or square wave is used to drive a LOW Pass Circuit the effect on the shape of the pulse is to see the R-C charge and discharge characteristic of the circuit. The theory is discussed in the experiment.

2.

LOW PASS R.C. "RESPONSE"

CAPACITANCE for R = 10K)	WAVEFORM	RISE TIME
330 pfd		10 μsec
.001 mfd		10 μsec
.01 mfd		$\frac{0.7}{50 \times 10^{-6}}$ = 14,000v/sec (measure rate in volts per second.)
.25 mfd	 (change scale on oscilloscope)	$\frac{0.1}{50 \times 10^{-6}}$ = 2,000v/sec

3. The circuits which exhibit a linear voltage sweep are the 0.01 mfd and the 0.25 mfd circuits.

RATE = 14,000 volts per second

LOW PASS R.C. CIRCUIT

$$\text{TIME CONSTANT (T)} = RC = (10^{4})(0.01 \times 10^{-6}) = 0.01 \times 10^{-2} = \underline{100 \text{ msec}}$$

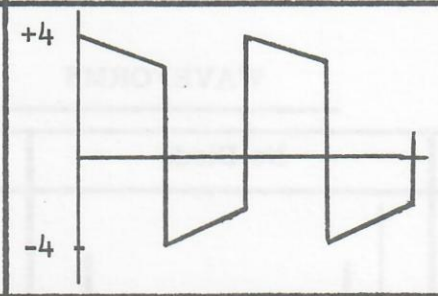
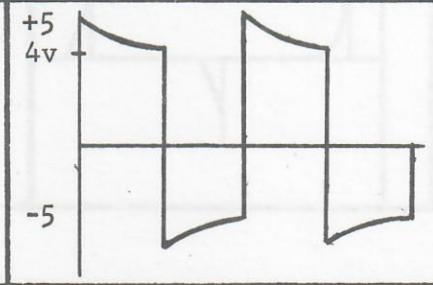
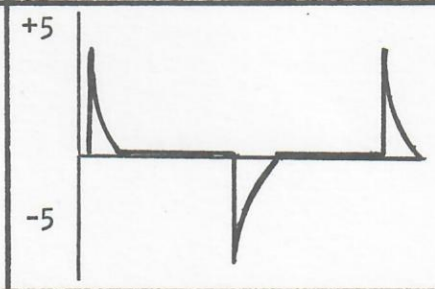
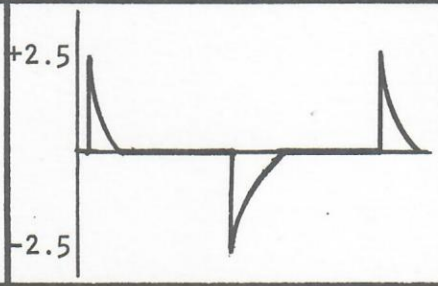
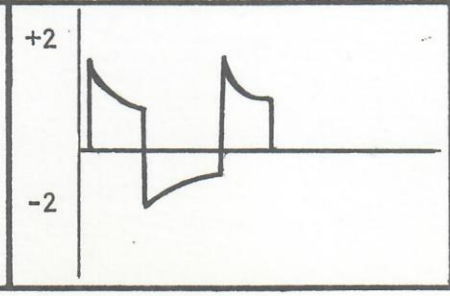
$$\text{RATE} = \frac{0.7}{100 \times 10\text{-}6} = 0.007 \times 10^{6} = 7{,}000 \text{ volts/second}$$

The actual measured rate is twice the calculated rate, perhaps due to circuit variations and measurement. The important point is that the student learn the principle used to generate a linear voltage sweep using an R-C network.

HIGH PASS R.C. CIRCUIT

When a HIGH PASS R.C. CIRCUIT is driven by a Square Wave or Pulse the effect will be for the circuit to pass the high frequency component or the rising and falling edges of the signal and to attenuate the low frequency part of the signal which is the Positive or Zero D.C. pulse levels.

2. R.C. HIGH PASS CIRCUIT

RESISTOR (CAP = 0.001 mfd)	WAVEFORM	COMMENTS
.1 MEGOHM		The output follows the edges of the waveform but tries to return to zero during the D.C. portion of the pulse.
100K		The R.C. discharge curve of the network can be seen during the D.C. portion of the pulse.
10K		Only the edges have the high frequency to "pass" the network. The capacitor fully discharges between pulses.
2.2K		The edges are passed as spikes, the short time constant is clearly seen.
R = 2.2K Use the capacitance between your hands.		The time constant of the hands results in a circuit reaction similar to the 100 K circuit.

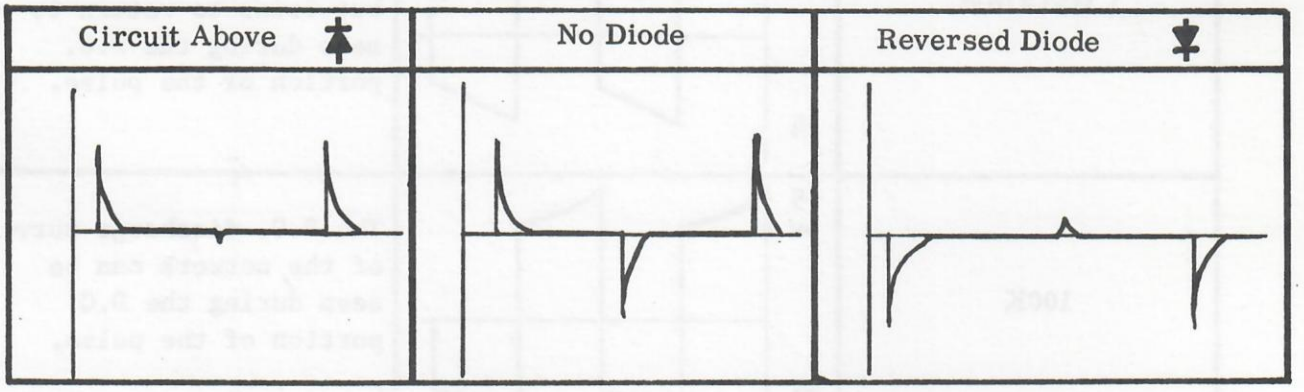
HIGH PASS R.C. CIRCUIT

3. The Voltage Droop is the amount the output voltage decrease after the initial voltage jump and before the next input pulse.

DROOP = 1 VOLTS	for 100K resistor

5.

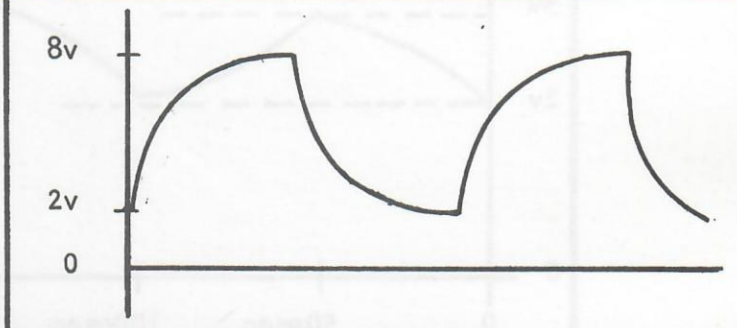
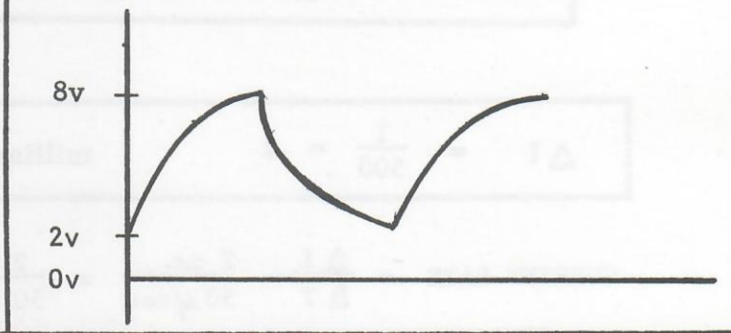
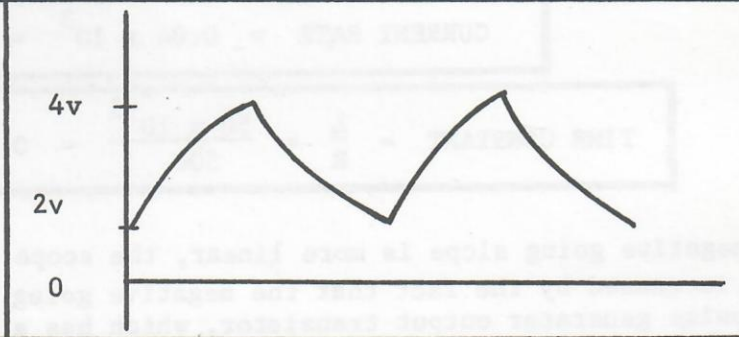
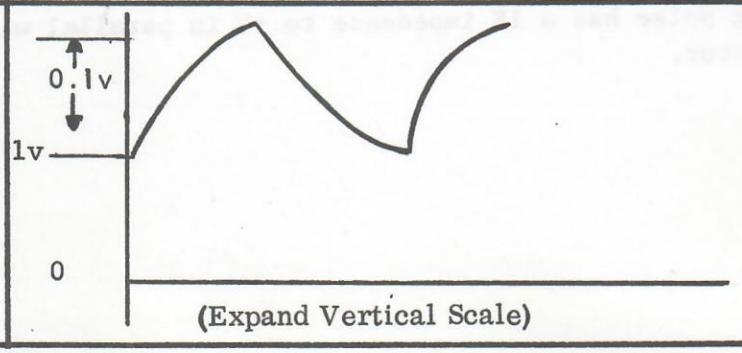
WAVEFORMS



LOW PASS R.L. NETWORK

In the LOW PASS R.L. Circuit the inductor is the frequency sensitive element. The inductor is a very high impedance for high frequencies.

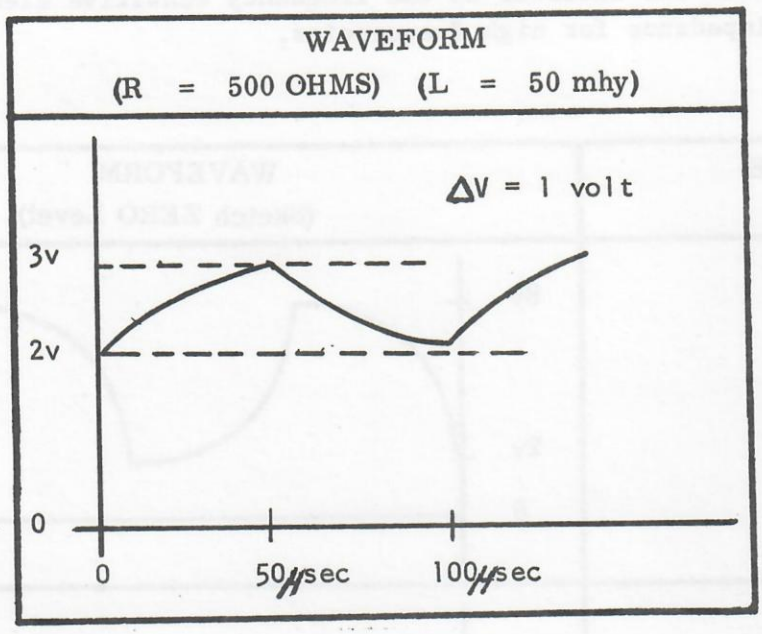
3. LOW PASS R-L NETWORK

RESISTANCE L = 50 mhy	WAVEFORM (Sketch ZERO Level)
10 K	
4.7K	
1K	
100 OHMS	

The most linear output waveforms occur for 1K and 100 ohm resistances.

LOW PASS R.L. NETWORK

4.



5.

$$\Delta I = \frac{1}{500} = 2 \text{ milliamperes}$$

6.

$$\text{CURRENT RATE} = \frac{\Delta I}{\Delta T} = \frac{2 \text{ ma}}{50\,\mu\text{sec}} = \frac{2 \times 10^{-3}}{50 \times 10^{-6}} = \frac{2}{50} \times 10^{3}$$

$$\text{CURRENT RATE} = 0.04 \times 10^{3} = 40 \text{ amperes/second}$$

7.

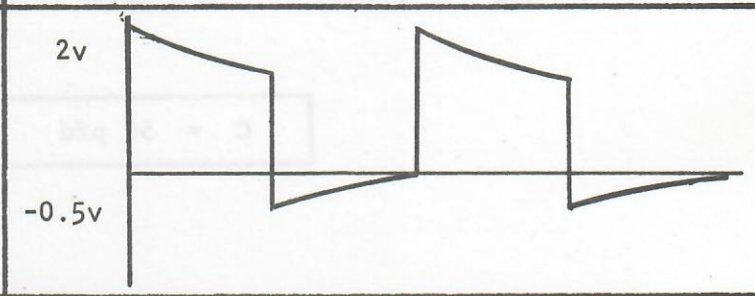
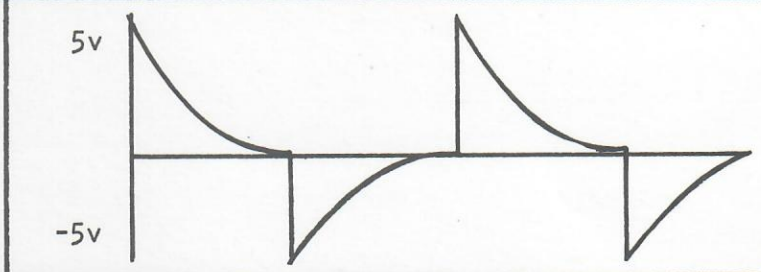
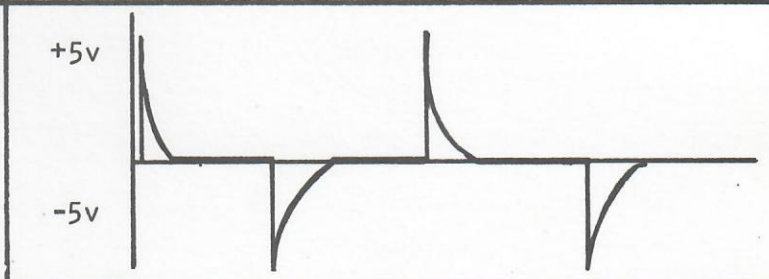
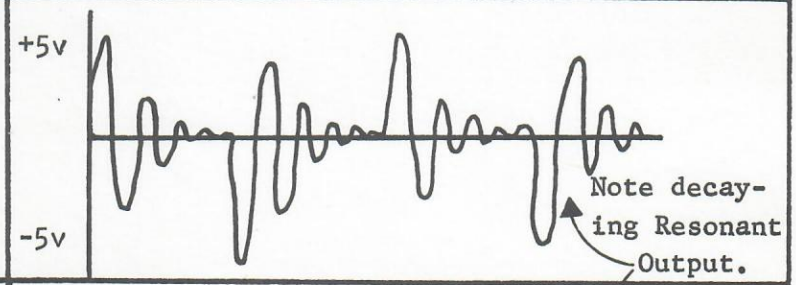
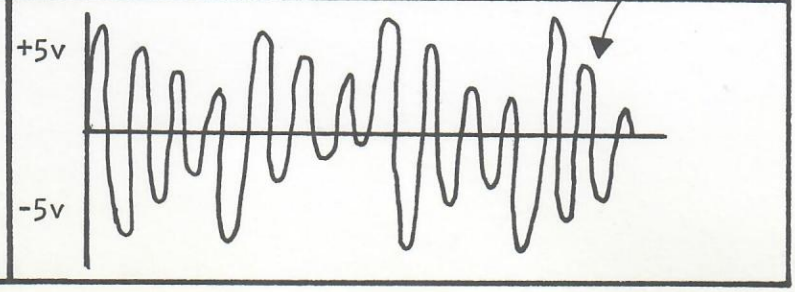
$$\text{TIME CONSTANT} = \frac{L}{R} = \frac{50 \times 10^{-3}}{500} = 0.1 \times 10^{-3} = 100 \text{ microseconds}$$

The negative going slope is more linear, the scope trace is more nearly a straight line. This is caused by the fact that the negative going pulse is connected to ground via the pulse generator output transistor, which has a very low impedance. The positive going pulse has a 1K impedance to +V in parallel with the 2.2K pulse generator pull up resistor.

HIGH PASS R-L NETWORK

The inductor has a high impedance for high frequencies, therefore the pulse edges, which are high frequency signals, will appear at the output. The inductor is a low impedance for low frequencies and D.C. voltages so the output during the peak and ground level of the pulse will be small.

3. HIGH PASS R-L CIRCUIT

RESISTANCE (L = 50 mhy)	WAVEFORM
100 OHMS	
2.2K	
10K	
100K	
1M	

HIGH PASS R-L NETWORK

4. PERIOD OF OSCILLATION = 10 microseconds

$$\text{FREQUENCY} = \frac{1}{10 \times 10^{-6}} = 0.1 \times 10^{6} = 100{,}000 \text{ Hertz}$$

5. Calculation of Stray Capacitance

$$C = \frac{1}{2f^2} = \frac{1}{2(10^5)^2} = \frac{1}{2 \times 10^{10}} = 0.5 \times 10^{-10} = 50 \text{ pfd}$$

$$C = 50 \text{ pfd}$$

SERIES L-C-R CIRCUIT

The circuit used is a Series Resonant Circuit. The resonant frequency is given by:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

for L = 50 mhy

C = 330 pfd

$$f = \frac{1}{2\pi} \quad \frac{1}{(50 \times 10^{-3})(330 \times 10^{-12})} = \frac{1}{2\pi} \quad \frac{1}{16{,}500 \times 10^{-15}}$$

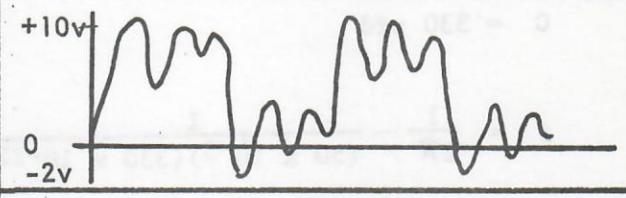
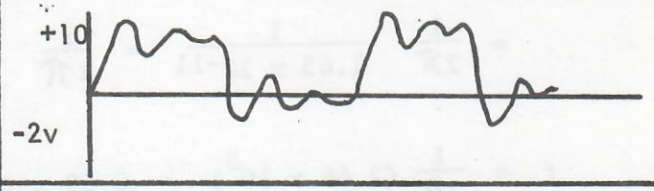
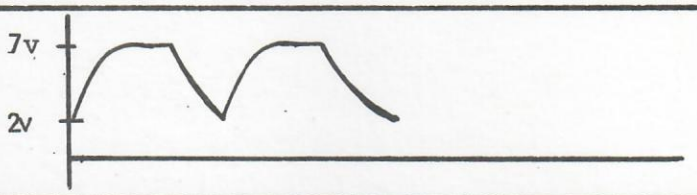
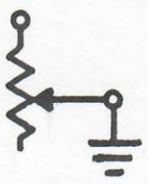
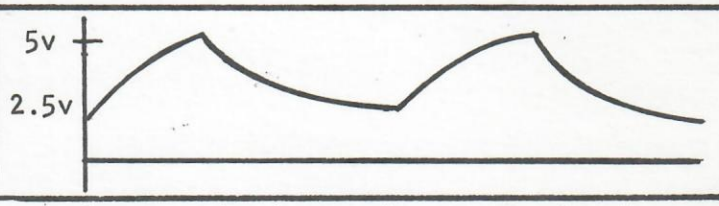
$$= \frac{1}{2\pi} \quad \frac{1}{1.65 \times 10^{-11}} = \frac{1}{2\pi} \quad 0.606 \times 10^{11} = \frac{1}{2\pi} \quad 6.06 \times 10^{10}$$

$$f = \frac{1}{2\pi} (2.46 \times 10^{5}) = 0.39 \times 10^{5} = 39 \text{ KHz}$$

Ringing or oscillation should occur at approximately this frequency. The purpose of this experiment is to demonstrate the use of a load resistor to damp or eliminate this oscillation.

SERIES L-C-R CIRCUIT

3. SERIES L-C-R CIRCUIT

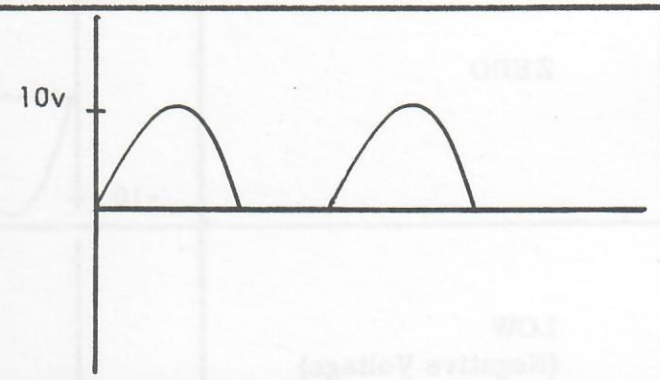
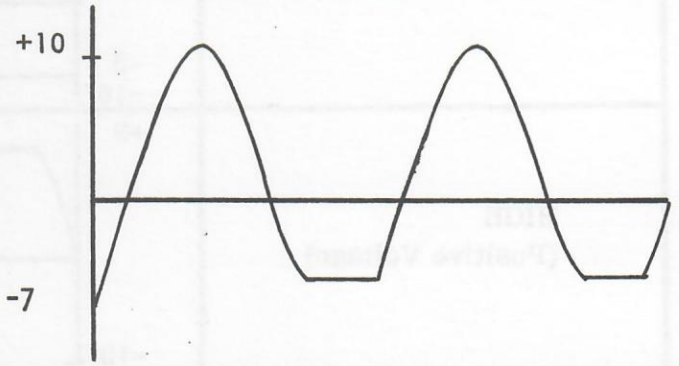
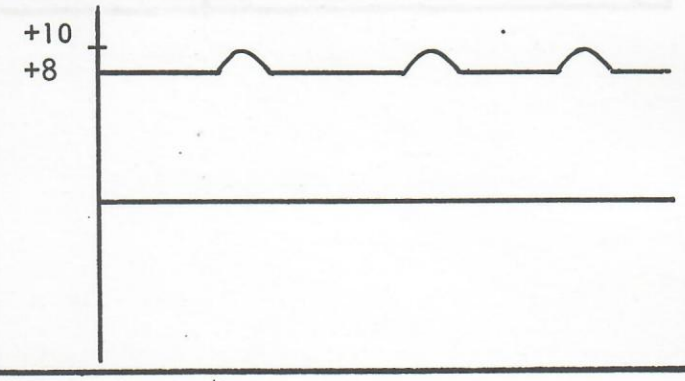
RESISTANCE	WAVEFORM
470K	
100K	
100K POT (Vary)	The oscillations increase for higher resistive values. The signal looks like a loaded pulse when the 100K POT is set at approximately 10K.
3.3K	
10K POT (Vary) 	At full 10K there is a small oscillation on the output signal. As the 10K is decreased the oscillation stops and the signal becomes more rounded.
1K	

4. A resistance in the order of 8K ohms yields the best square wave output.

SERIES DIODE CLIPPERS

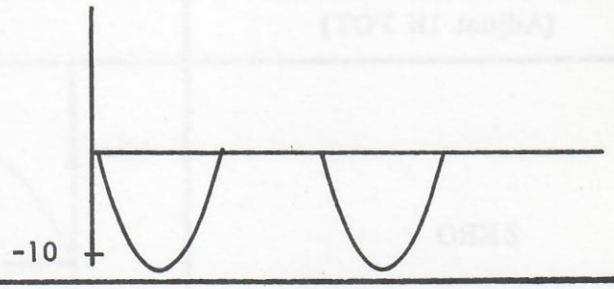
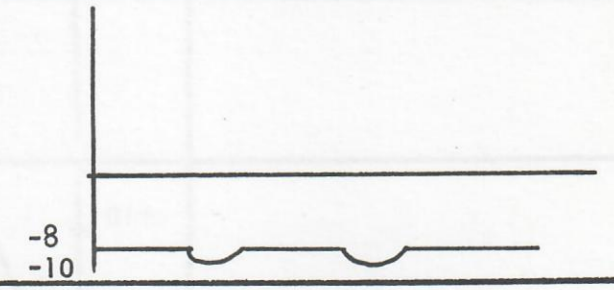
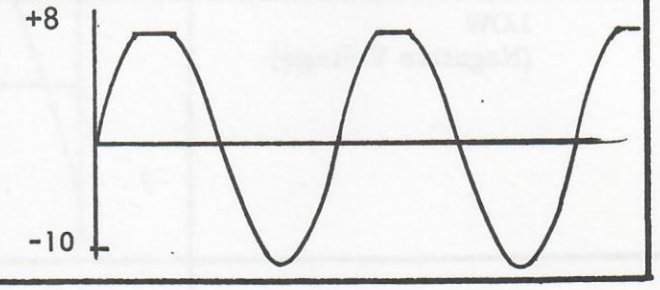
The diode D4 in the circuit will not turn ON until the input voltage from the transformer is larger than the voltage on the diode cathode. Therefore the portion of the input waveform that is a lower voltage than the voltage set on the wiper of the 1K POT will be cut off or "clipped". Only the portion of the waveform greater then the POT voltage will appear at the output.

4.

CLIPPING LEVEL (Adjust 1K POT)	WAVEFORM (Positive Series Clipper)
ZERO	
LOW (Negative Voltage)	
HIGH (Positve Voltage)	

SERIES DIODE CLIPPERS

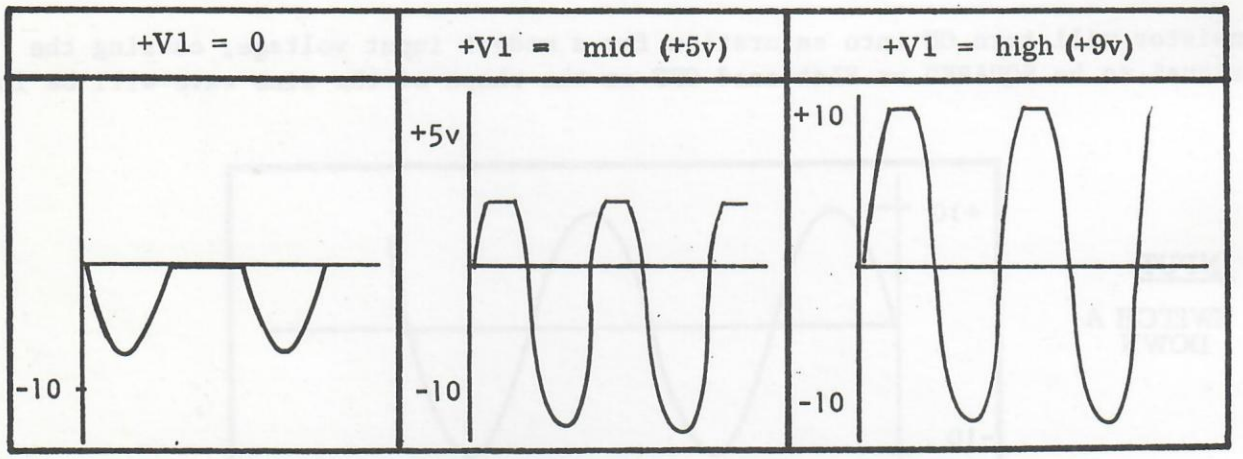
6.

CLIPPING LEVEL (Adjust 1K POT)	WAVEFORM (Negative Series Clipper)
ZERO	
LOW (Negative Voltage)	
HIGH (Positive Voltage)	

SHUNT DIODE CLIPPERS

In this circuit, when the output voltage exceeds the value of the variable voltage on the cathode of the diode the diode will turn ON and prevent the output voltage from increasing beyond that point.

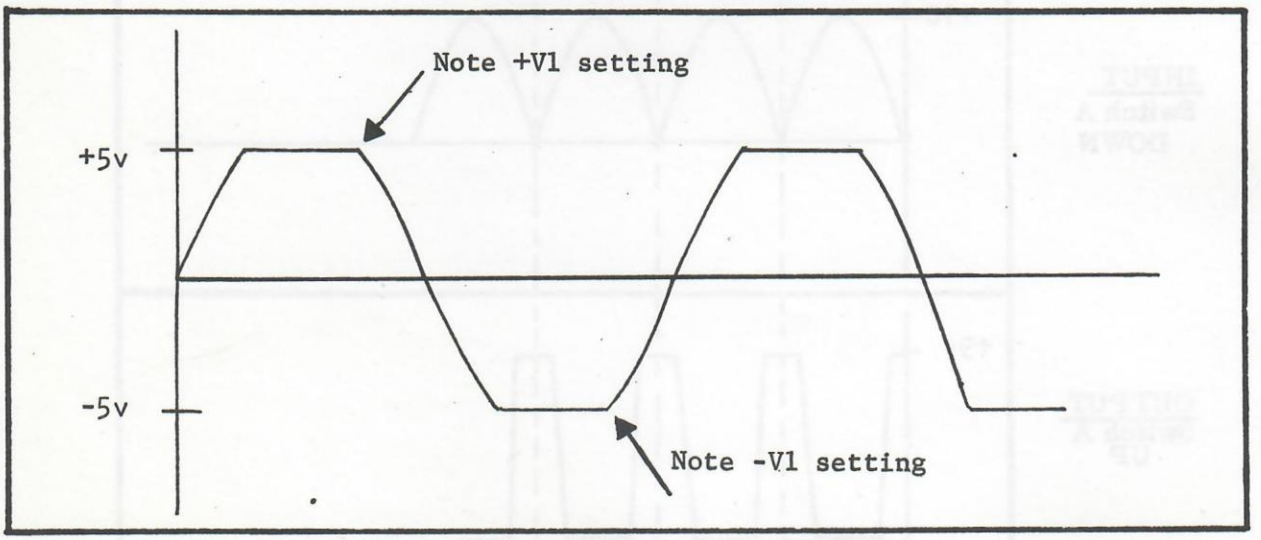
3.



4. The NEGATIVE SERIES DIODE CLIPPER will produce the same waveforms as this Shunt Diode Clipper.

5. The adjustment of -V1 controls the clipping voltage level of the negative half cycle of the signal. The +V1 controls the clipping level of the positive half cycle.

6.

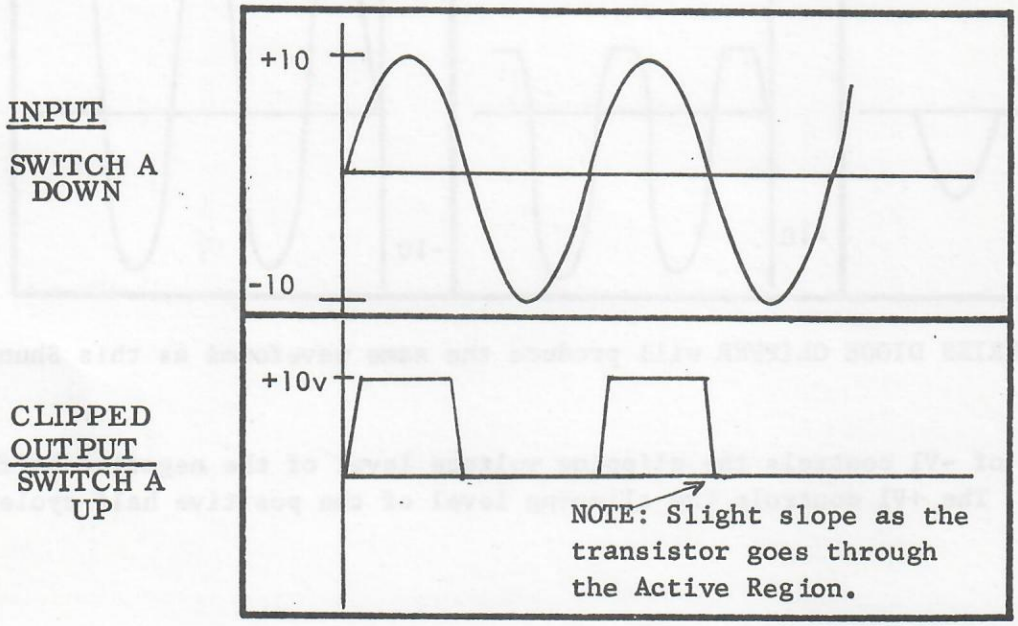


TRANSISTOR CLIPPER & SQUARER

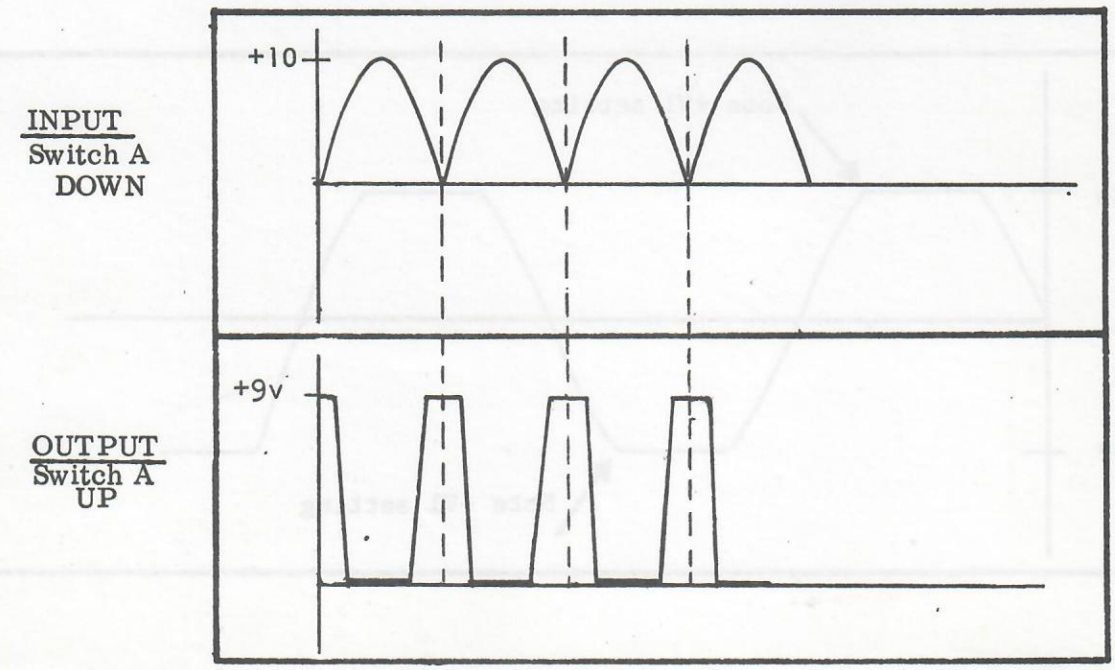
The transistor collector output will provide only positive output voltages. For negative voltage inputs the transistor will be OFF and the output voltage will be +V2. For positive input voltages the transistor will be saturated and the output will be very nearly ground.

The transistor will turn ON into saturation for a modest input voltage, causing the output signal to be SQUARED or Flattened OFF so the shape of the sine wave will be lost.

2.



4.

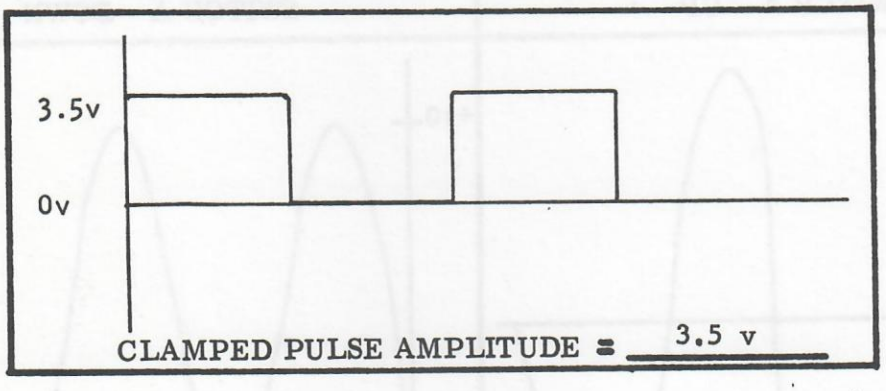


The frequency of the output pulses is 120 Hz. There is one positive pulse for each zero crossing of the input signal (2 per cycle).

DIODE PULSE CLAMPING

The Zener Diode limits the Positive Pulse Amplitude to approximately 3.5 volts. When the collector voltage of Q5 is larger than the Zener Voltage, D5 will turn ON and clamp the output voltage to the Zener Voltage. When the output voltage is loaded, no effect will be seen on the Output Voltage Amplitude until the load pulls the Collector voltage below the Zener Voltage.

2.



CLAMPED PULSE AMPLITUDE = 3.5 v

3.

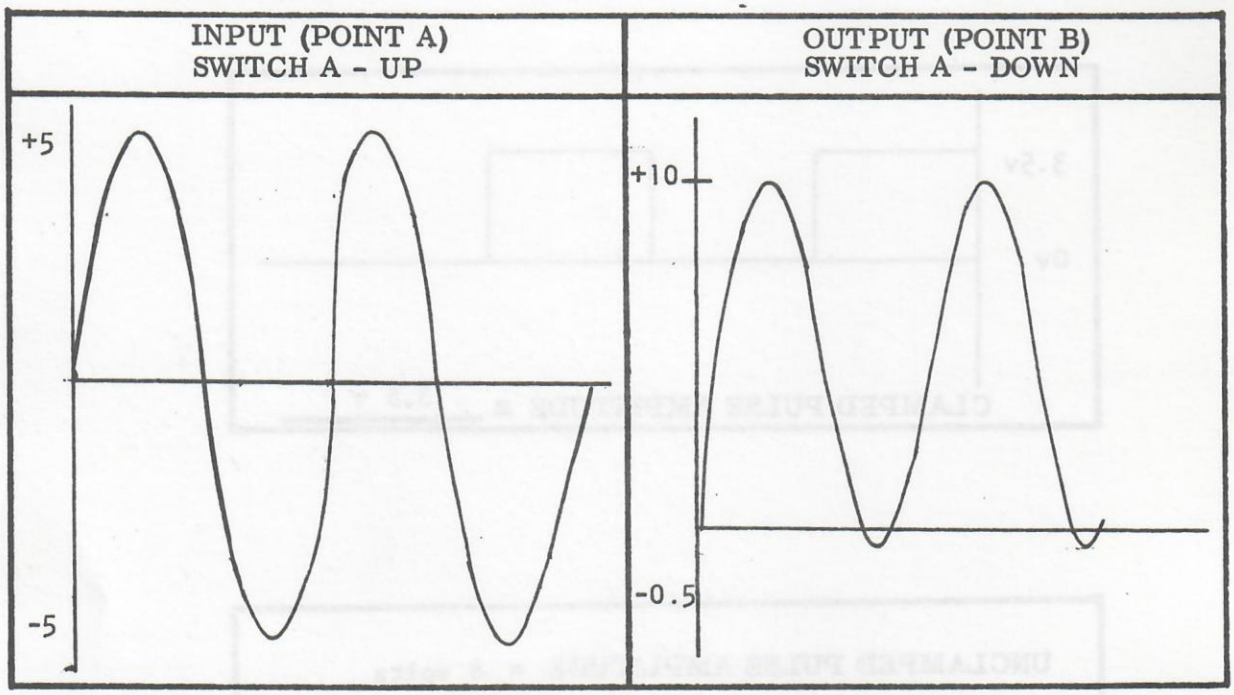
UNCLAMPED PULSE AMPLITUDE = 8 volts

An application of this circuit would be in a Square Wave Signal Generator where the output amplitude must be constant for different loads.

D.C. RESTORER

This circuit is useful when it is required to convert an A.C. signal to a Positive only A.C. signal. One example that could be used is that, if a D.C. Meter were connected to the output the meter reading will be proportional to the Average Amplitude of the A.C. Signal.

2.



3. When V1 is varied, the D.C. level of the output varies.

4. The output waveform A.C. amplitude is the same as the Input A.C. amplitude. The D.C. level is adjusted so that the negative peak of the A.C. waveform is at ground.

A.C. SOLID-STATE VOLTMETER

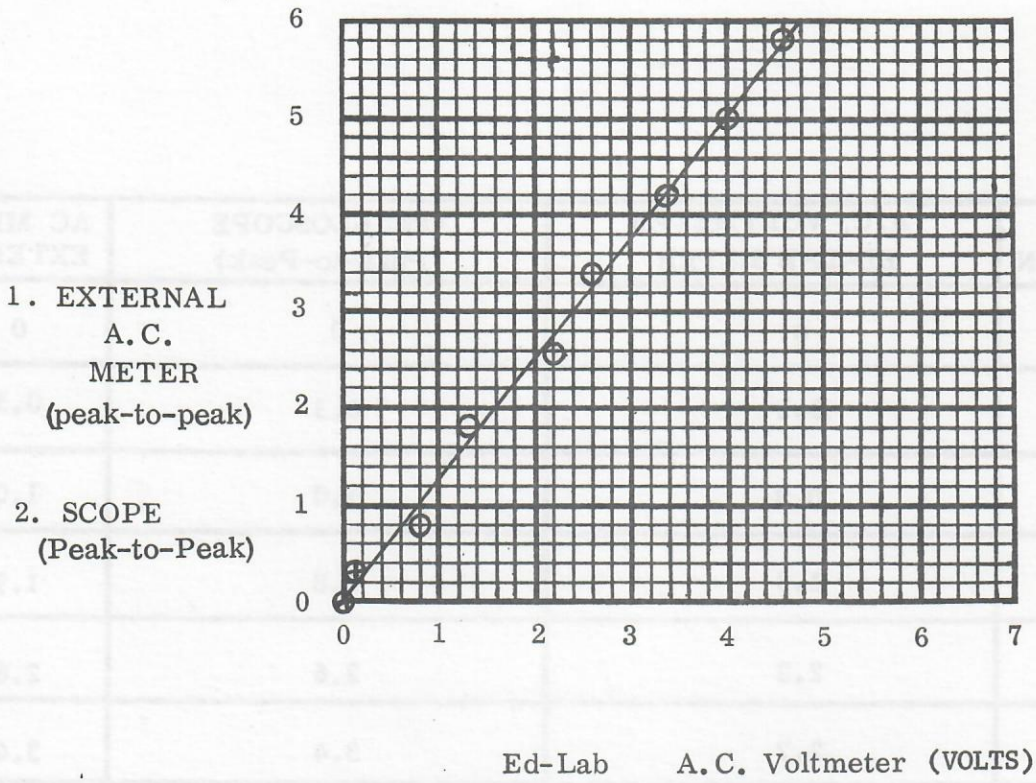
This is a practical application of the D.C. Restorer as used to implement an A.C. Meter. Note the use of the Emitter Follower circuit to prevent loading by the Voltmeter.

5.

POT POSITION	A.C. VOLTMETER ED-LAB METER	OSCILLOSCOPE (Peak-to-Peak)	AC METER EXTERNAL
0	0	0	0
1	0.1	0.3	0.3
2	0.8	1.0	1.02
3	1.3	1.8	1.9
4	2.2	2.6	2.6
5	2.7	3.4	3.4
6	3.4	4.2	4.2
7	4.0	5.0	5.0
8	4.6	5.8	5.9
9	5.7	6.4	6.4
10	6.0	7.0	7.0

A.C. SOLID-STATE VOLTMETER

5.

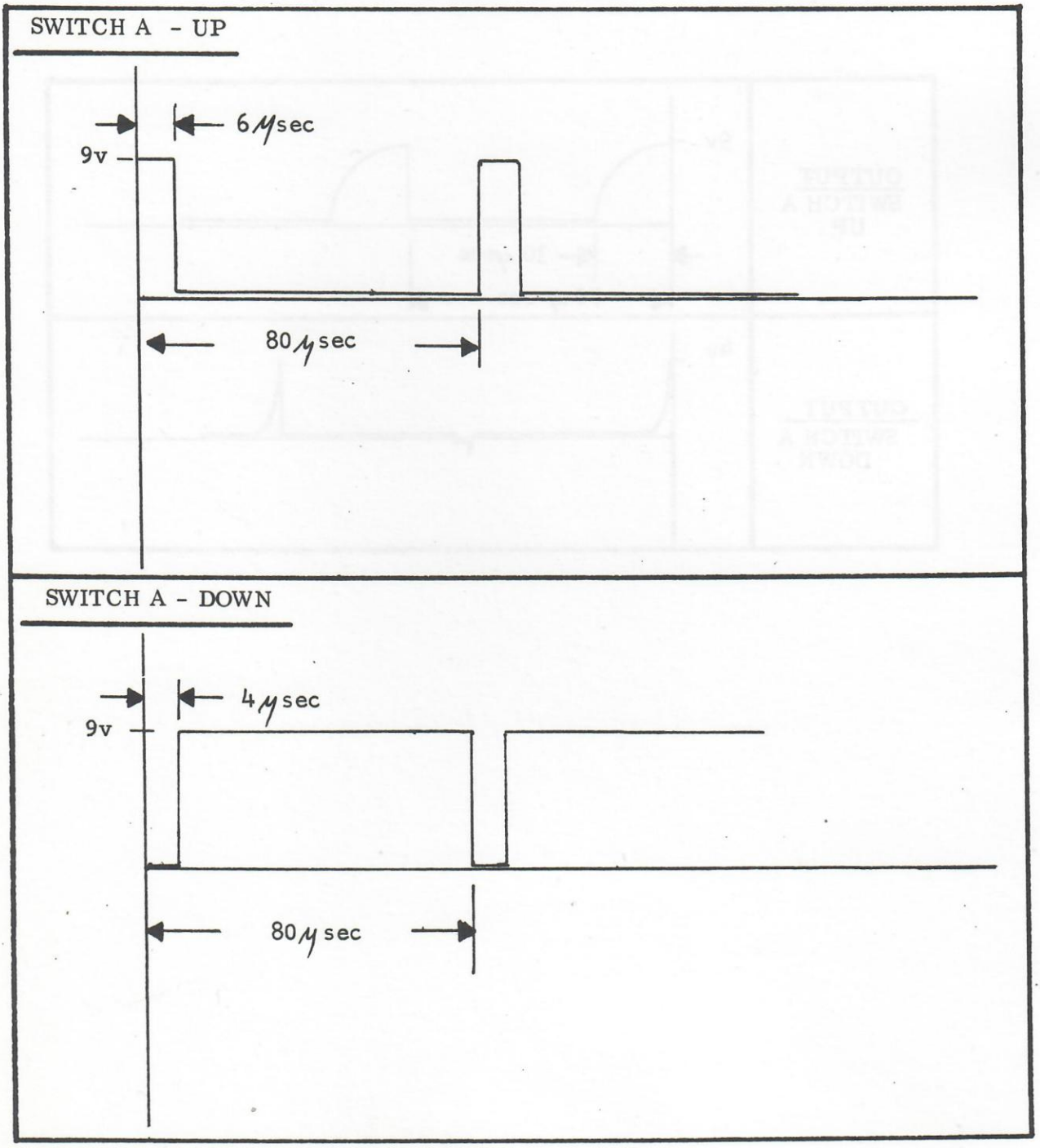


6. The waveform is distorted by the D.C. Restorer and the negative peak of the waveform is not clamped to zero. These factors result in the Average Voltage reading being different from the true RMS or Peak meter readings.

PULSE COMPRESSOR

The Pulse Compressor is a circuit used to generate a short positive or negative pulse at the leading or trailing edge of the input pulse.

3. PULSE COMPRESSOR OUTPUTS

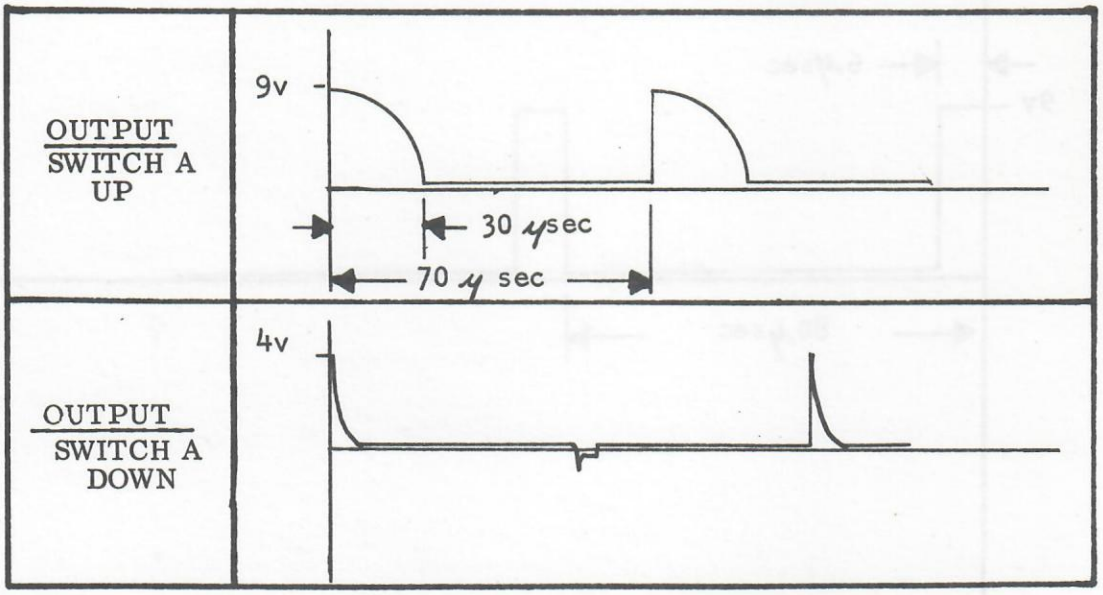


4. Switch A - UP is the Lagging Edge One Shot
   Switch A - DOWN is the leading Edge One Shot

PULSE STRETCHER

The Pulse Stretcher circuit is used to lengthen the time duration of very sharp input pulses. The lengthened pulse is more reliable for use as a drive signal.

3.



PULSE STRETCHER

4.

1M POT SETTING	PULSE WIDTH
100K	15 microseconds
200K	30 microseconds
300K	40 microseconds
400K	50 microseconds*
700K	pulses do not return to zero volts for higher POT settings
900K	pulses do not return to zero volts for higher POT settings

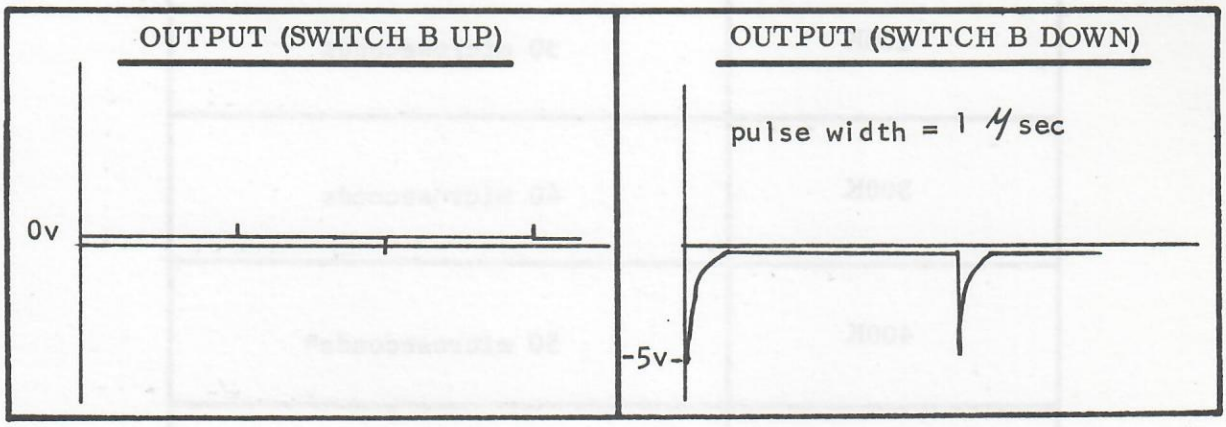
5. What happens as R increase (POT Resistance)?

The pulses will become longer as R increases because the RC time constant will increase. Above a critical value of R the Transistor Q5 will not turn ON because the base current will not be large enough ($I_B = \frac{V1}{R}$) to generate enough Collector current to pull the collector down to Zero. The "low" level of the output pulse will not reach zero.

CAPACITOR-DIODE GATE

The Capacitor-Diode gate is used to control the transmission of pulses. The gate can either pass or block input pulses to a following stage.

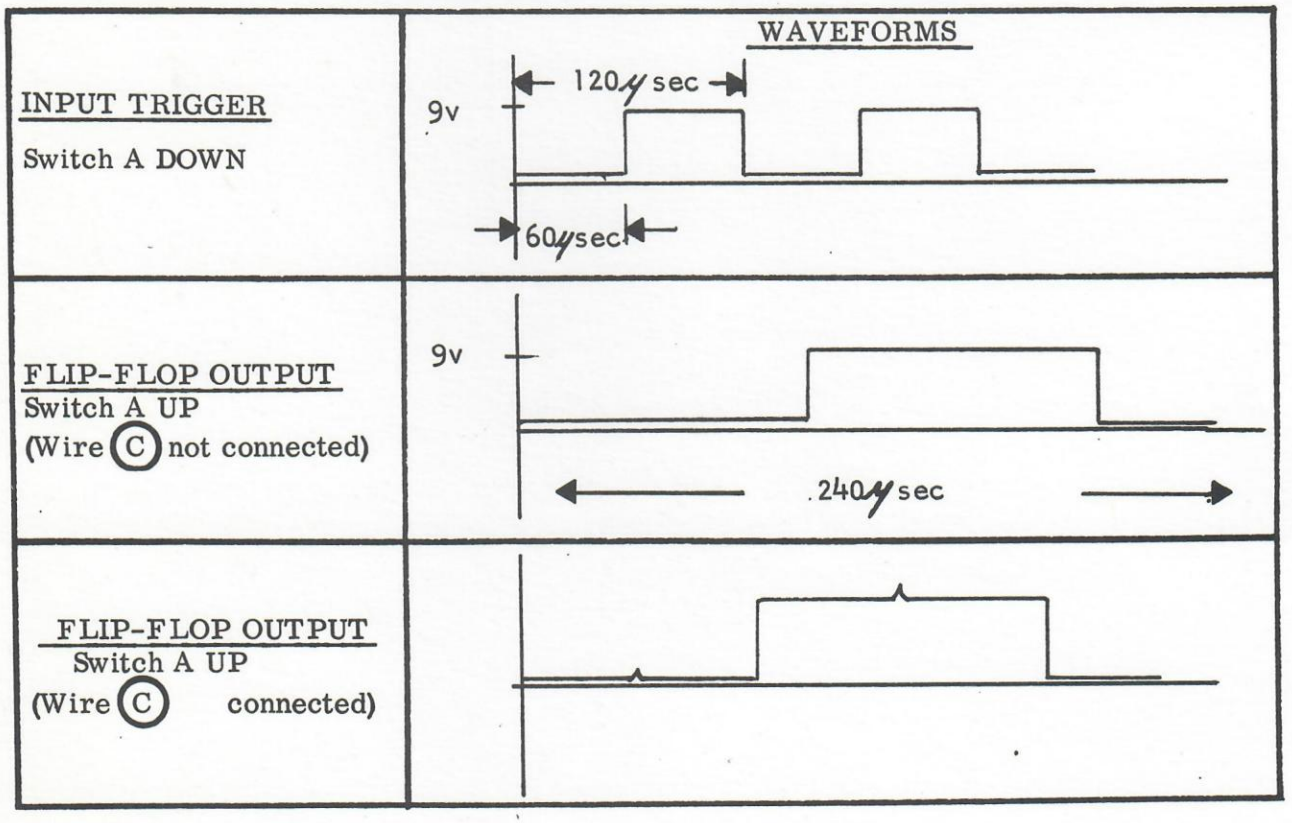
2. Waveforms



TRIGGERED FLIP-FLOP

The Bistable Flip-Flop circuit of Experiment No. 2 is used. Added to this basic circuit are two Capacitor Diode gates, one driving the base of each transistor. When a C-D gate is ON (passing the negative pulses) the base of that transistor will be pulsed to ground and the output of that transistor will assume a "1" or "High" voltage level. Note that when the connection A and B are made the circuit will switch with each trigger pulse. This is called the "Toggle" or "Trigger" mode of operation. If the J and K gate controls are connected to an external circuit then the Flip-Flop may be"steered" to a particular state by setting a "0" on the control for the transistor output to be set to a "High". Note that the Flip-Flop will follow the J and K inputs when the next trigger pulse occurs. This is call "synchronous operation" because the change in the Flip-Flop is synchronized to the trigger pulse.

2.



3. From the observations on the oscilloscope, which input edge triggers the flip-flop?

The Flip-Flop changes state at the instant that the negative trigger superimposed on the square wave occurs. The negative going edge triggers the Flip-Flop.

STAIRCASE GENERATOR

The positive pulses from the collector of Q4 each charge the 0.25 μfd capacitor to a slightly higher voltage, creating a staircase or step increasing voltage output. When the Unijunction transistor fires the capacitor discharges and the output returns to zero.

The amount that the capacitor voltage will increase for each pulse is given by:

$$v = \frac{1}{c}\int_0^t i\,dt \qquad \text{where} \qquad i = \frac{V1 - Vy}{15K}$$

in the case of a square pulse we can very easily perform the integration.

$$v = \frac{1}{c}\left[\frac{V1 - Vy}{15K}\right] T_p$$

where T_p is the duration of the position pulse in seconds.

STAIRCASE GENERATOR

3. Waveforms

STAIRCASE GENERATOR

4.

	(Use Oscilloscope)
NUMBER OF STEPS	5
PERIOD	2.0 m sec
STEP-SIZE (Volts)	0.5 volts (step 1) 0.4 volts (step 5)
VOLTAGE SWING	1 volt to 3 volts

5. Does the PERIOD change when the frequency is varied?

The PERIOD does not change when the frequency is varied (1K POT adjustment changed). The number of steps in each sweep will change with frequency. The higher the frequency the larger the number of steps in each cycle.

6. What circuit components determine the PERIOD?

The circuit components which effect the Period are:

a. The 15K collector resistor of Q4. The value of this resistance will control the amount of current provided to the capacitor which will control the size of each voltage step of the capacitor. The larger the resistance, the smaller the current. This will then require more current pulses to charge the capacitor to the Unijunction firing voltage which will change the period of the ramp.

b. The value of the capacitor connected at the cathode of D1 will effect the period of the waveform. The voltage step caused by each current pulse is inversely proportional to the capacitance. Therefore if the size of the capacitor is increased the voltage step will decrease and more pulses will be required to reach the Unijunction firing voltage so the period will decrease.

7. What determines the number of steps?

The number of steps is controlled by the input frequency, the size of the capacitor and the value of the Q4 collector resistor.

Input Frequency: As the input frequency increases, the number of steps will increase.
Capacitance: As the capacitance increases the number of steps will increase.
Q4 Collector Resistor: As the resistance increases the number of steps will increase.

These three parameters will change the number of steps. Note that a change to the Q4 resistance or the Capacitor will also change the Period of the waveform. The input frequency, however, will change the number of steps without changing the Period of the waveform.

STAIRCASE GENERATOR

8. What determines the step voltage-amplitude?

   The step voltage amplitude is controlled by the input frequency, the Q4 collector resistor and the value of capacitance used. Note that the step size can be varied without changing the Waveform Period only by changing the input frequency.

9. What determines the voltage-swing?

   The voltage swing is determined by the firing voltage of the Unijunction Transistor.

10. What are the maximum and minimum number of steps that can be obtained?

    Without changing any of the circuit values the input frequency may be adjusted to obtain:

    MAXIMUM No. OF STEPS = 70

    MINIMUM No. OF STEPS = 1

11.

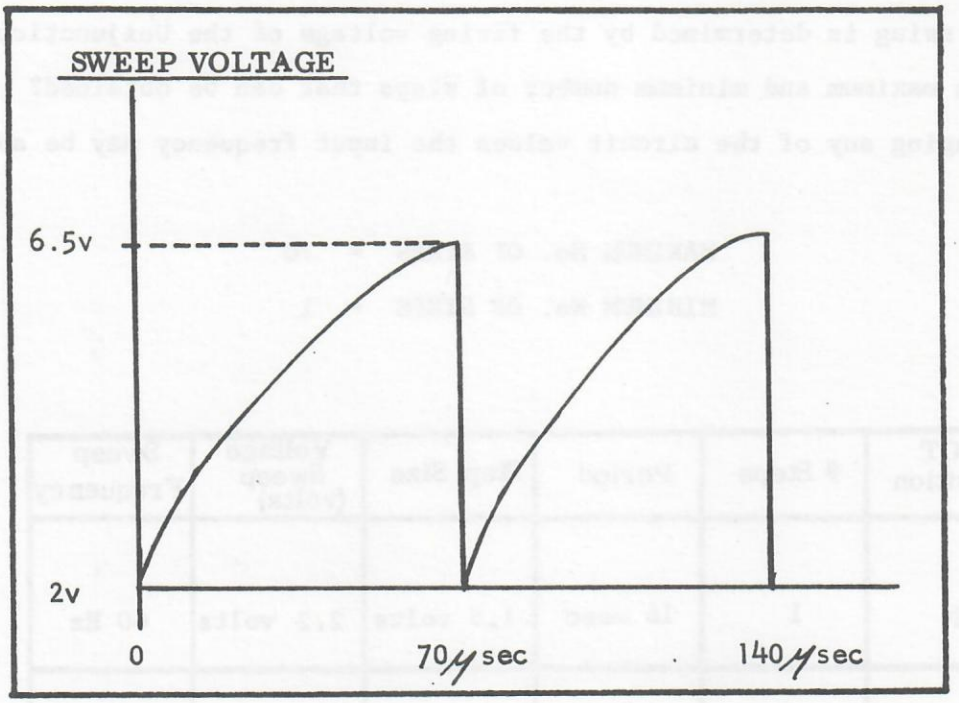
POT Position	# Steps	Period	Step Size	Voltage Sweep (volts)	Sweep Frequency
MIN	1	16 msec	1.5 volts	2.2 volts	60 Hz
MID	17	140 msec	0.15 volt	2.2 volts	7.1 Hz
MAX	* 22	350 msec	0.1 volts	2.2 volts	2.86 Hz

NOTE: The number of steps for the MAX Pot setting is difficult to measure because the sweep is very slow. The number 22 was arrived at by dividing the sweep voltage by the step size in volts.

UNIJUNCTION SWEEP CIRCUIT

The Unijunction Oscillator Circuit is fabricated and tested. In particular the output frequency and the amplitude and the Linearity of the sweep generated are recorded.

2.



UNIJUNCTION SWEEP CIRCUIT

3. Time Constant

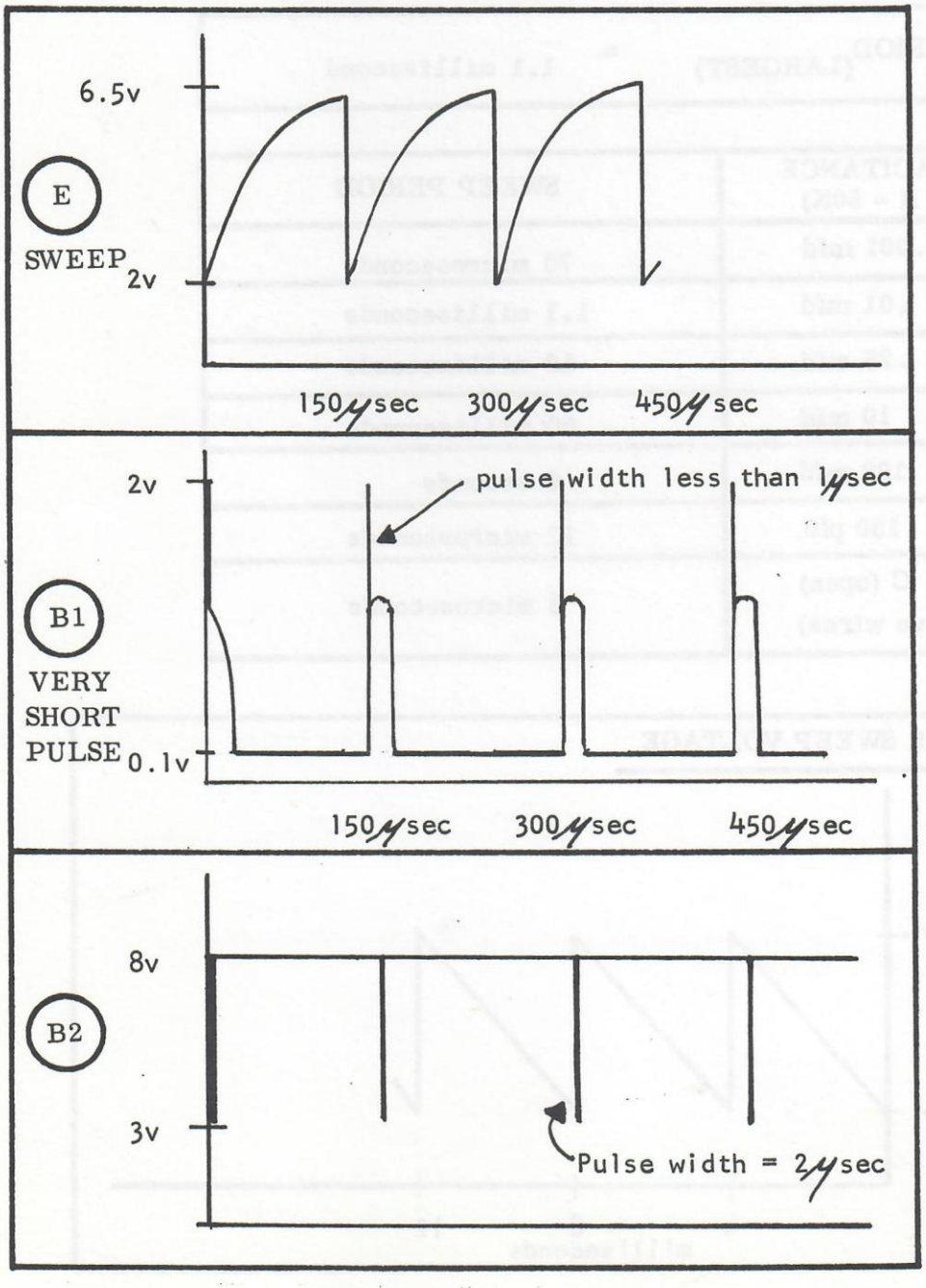
$$\tau = RC$$

$$\tau = (50 \ 10^{3}) \ (.001 \ 10^{-6})$$

$\tau =$ 50 (Microseconds)

4. The waveform Period is 1.5 times the RC Time Constant.

WAVEFORMS



UNIJUNCTION SWEEP CIRCUIT

5.

$R_{(LOWEST)}$	=	10 K ohms

$PERIOD_{(LOWEST)}$	=	14 μsec

6.

$R_{(LARGEST)}$	=	1 megohms

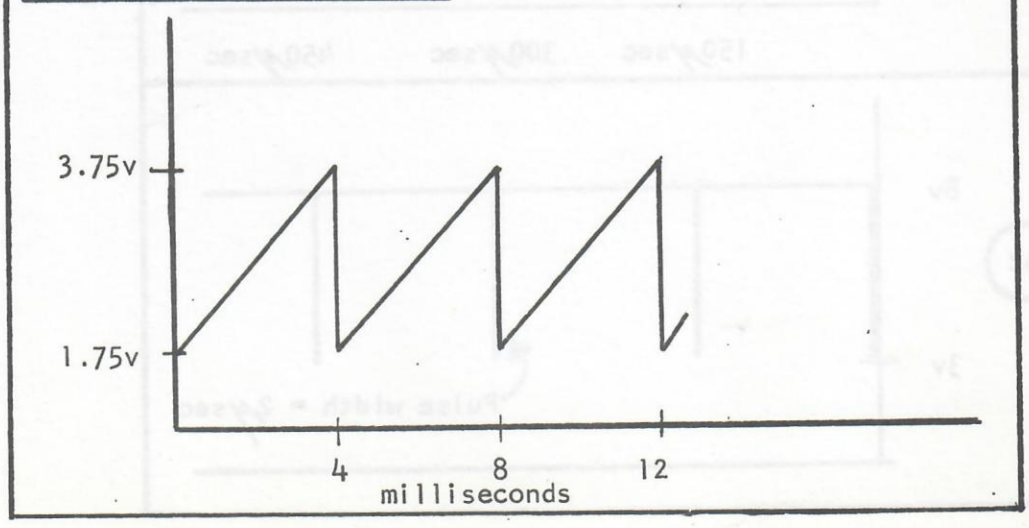
$PERIOD_{(LARGEST)}$	=	1.1 millisecond

7.

CAPACITANCE (for R = 50K)	SWEEP PERIOD
.001 mfd	70 microseconds
.01 mfd	1.1 milliseconds
.25 mfd	12 milliseconds
10 mfd	60 milliseconds
100 mfd	6 seconds
150 pfd	12 microseconds
C (open) (remove wires)	3 microseconds

8.

LINEAR SWEEP VOLTAGE



UNIJUNCTION SWEEP CIRCUIT

The sweep voltage is much more linear for the step 8 circuit.

9.

Measure

ΔV = 0.7 volts
V_m = 5 volts

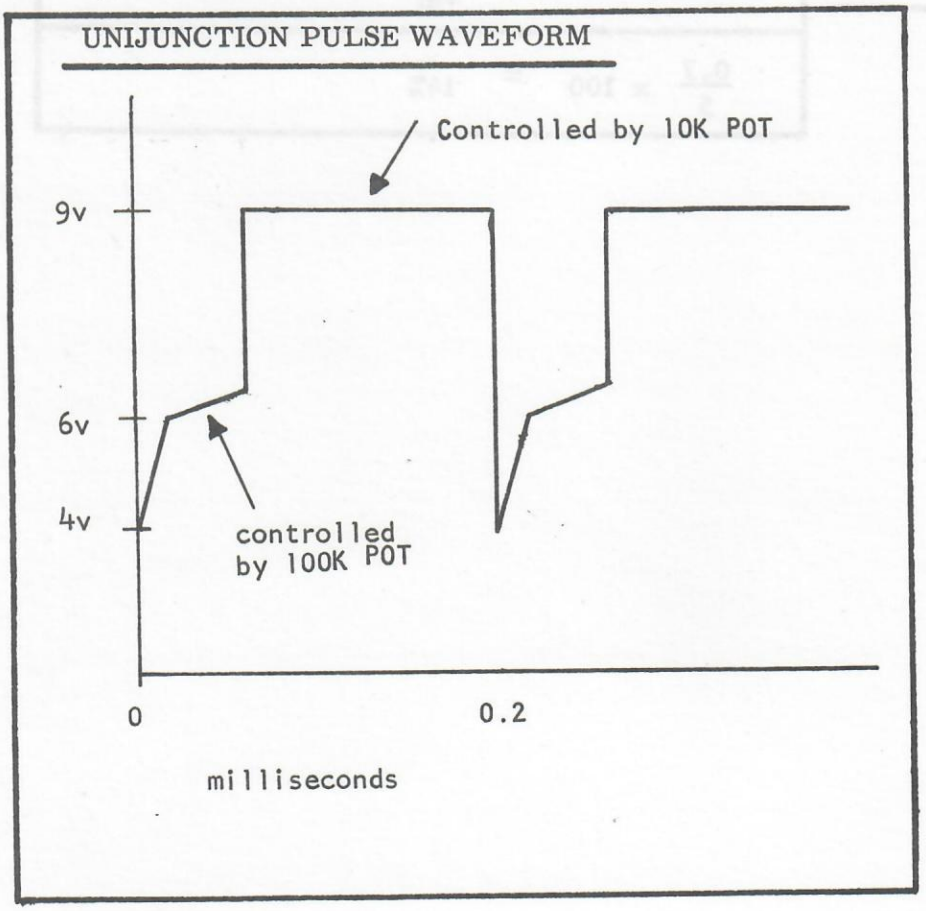
Calculate

Non-Linearity = $\frac{V_m}{}$ x 100%
$\frac{0.7}{5}$ x 100 = 14%

UNIJUNCTION PULSE GENERATOR

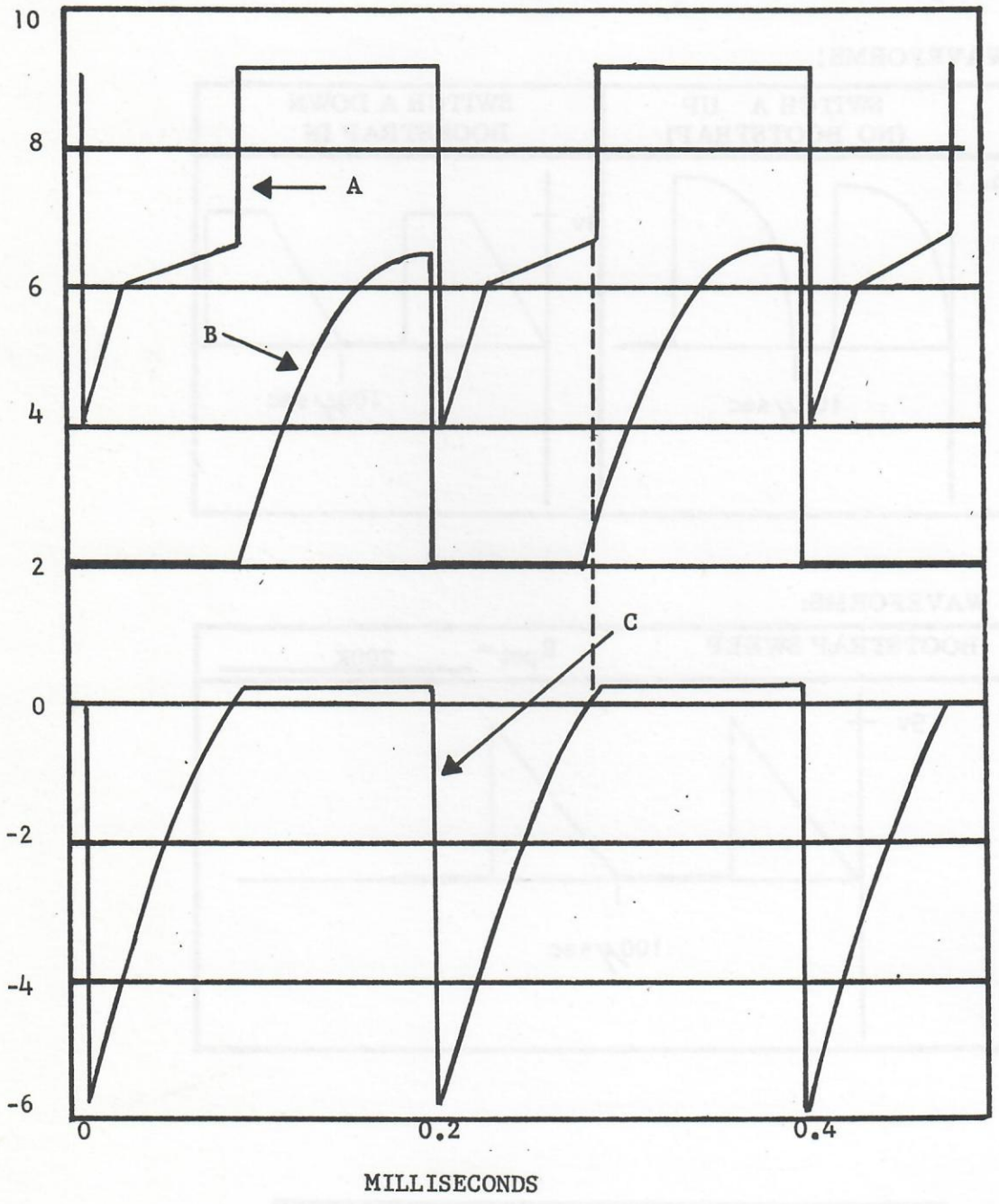
The Unijunction Pulse Generator Circuit takes advantage of different capacitor charging and discharging circuits to allow control of the positive and the negative duration of the pulse cycle. The secret to understanding the reason why there are different paths for charging and discharging is to note that when the Unijunction Transistor fires point B becomes zero and the voltage on the capacitor is applied to the Anode of the Diode D1. This voltage is negative and turns OFF the diode, blocking the normal discharge path of the capacitor and forcing the capacitor to discharge through the discharge circuit.

2.



UNIJUNCTION PULSE GENERATOR

3. Unijunction Output Waveforms

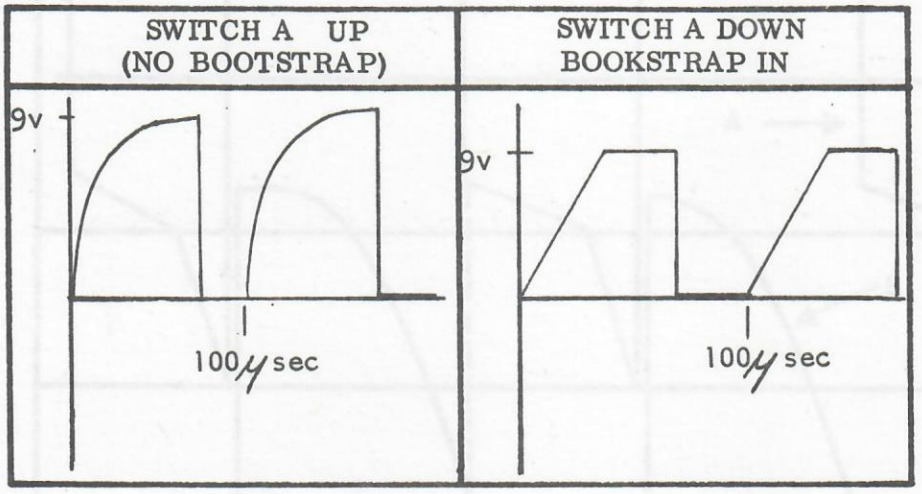


BOOTSTRAP SWEEP CIRCUIT

This circuit demonstrates the use of "feedback" to Linearize" the voltage output of a circuit. The circuit output is coupled to the capacitor drive circuit so the increasing output voltage will help to charge the capacitor and will make the capacitor voltage increase linearly.

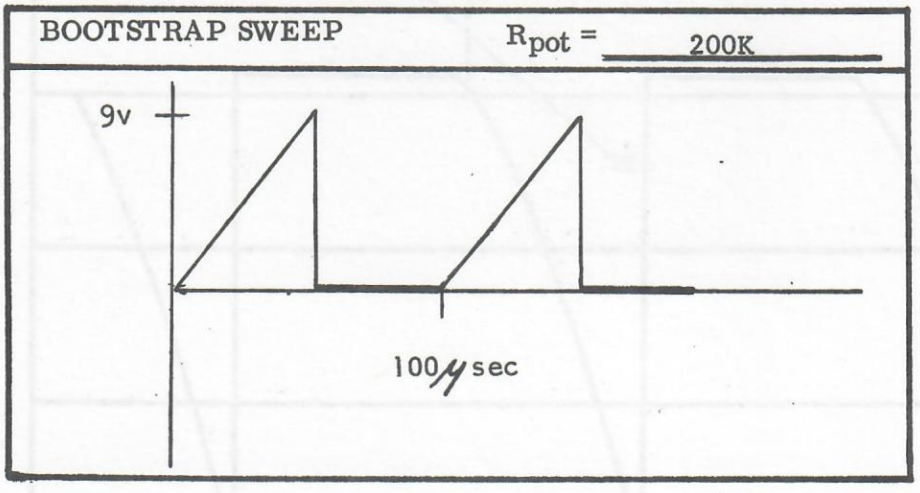
4.

WAVEFORMS:



5.

WAVEFORMS:

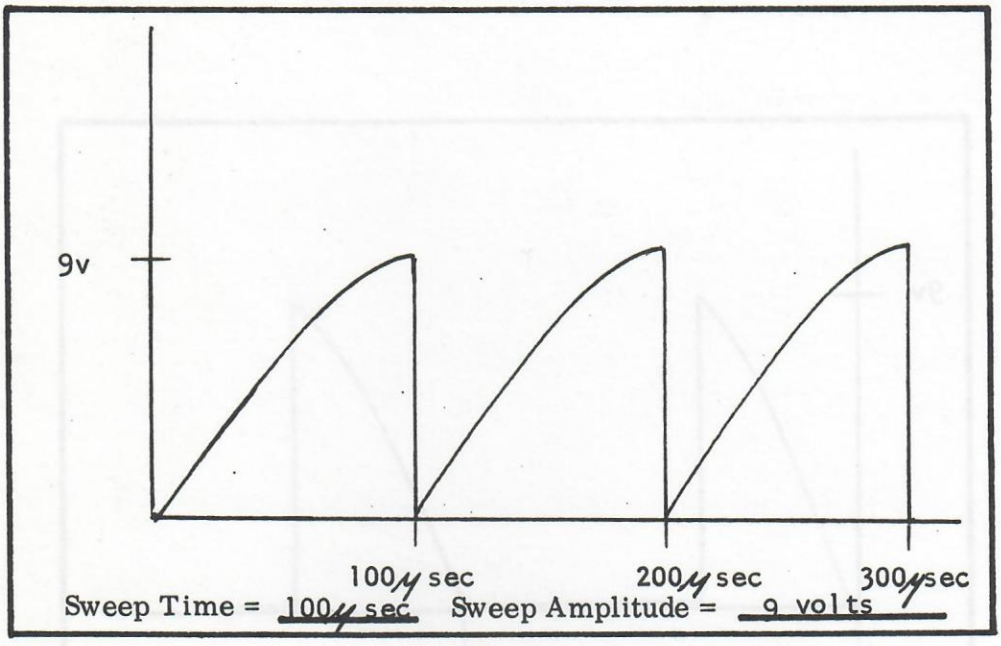


6.

$$\text{RATE} = \frac{9v}{50\mu\text{sec}} = 0.18 \text{ volts}/\mu\text{sec}$$

BOOTSTRAP SWEEP CIRCUIT

8. Waveform



Sweep Time = 100μ sec. Sweep Amplitude = 9 volts

9.

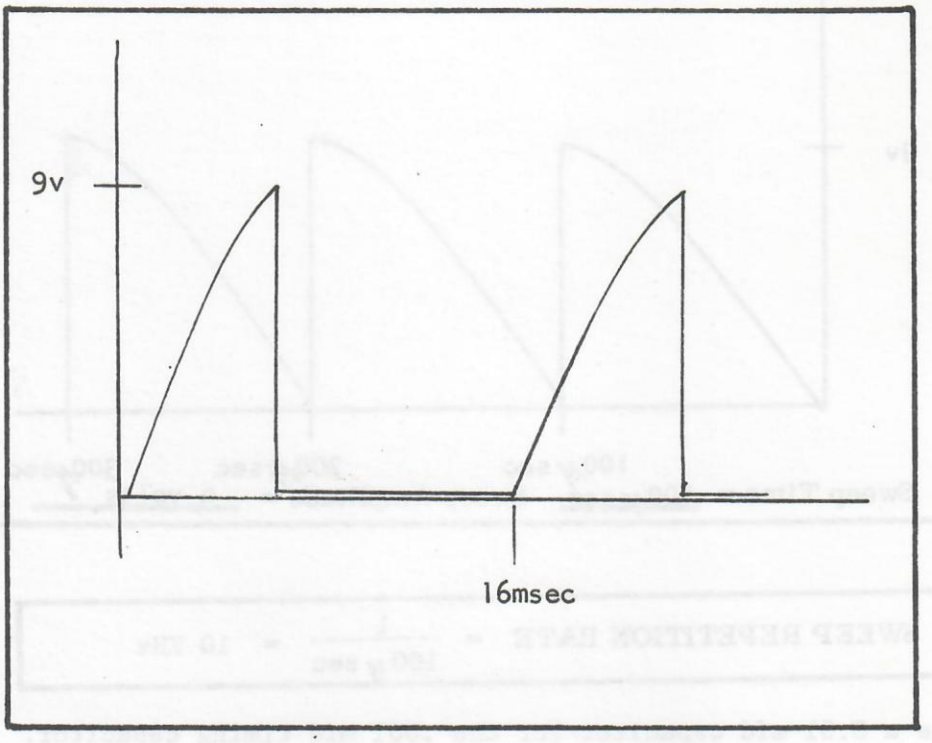
$$\text{SWEEP REPETITION RATE} = \frac{1}{100\mu\text{ sec}} = 10\text{ KHz}$$

10. Substitute a 0.01 mfd capacitor for the .001 mfd timing capacitor. What is the comparison with this larger capacitor in linearity, sweep period or rate, and sweep amplitude?

With the large capacitor the sweep linearity is improved, the sweep rate is the same and the sweep amplitude is 1/3 the 0.001 mfd capacitor or 3 volts.

BOOTSTRAP SWEEP CIRCUIT

12. Waveshape

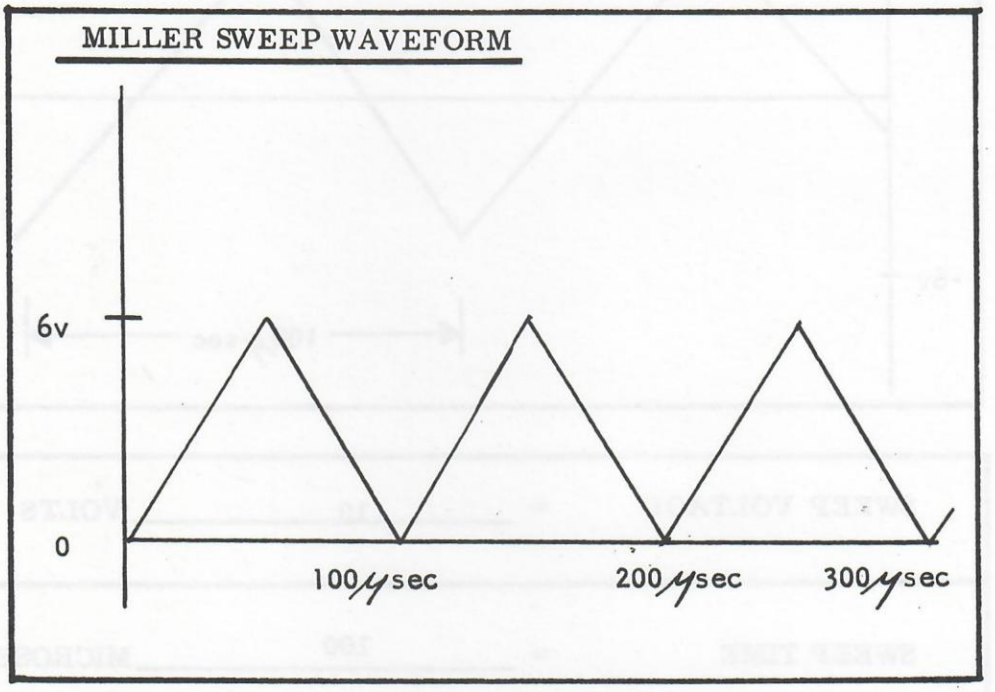


Note that a linear sweep voltage of this type can be used to generate an oscilloscope sweep rate synchronized to the 60 Hz A.C. Power Signal.

MILLER SWEEP

In this circuit the system has "negative feedback" where the increasing base voltage causes a decreasing collector voltage which is coupled to the base circuit via the 0.001μfd capacitor and decreases the amplifier gain. A result of the non-linear feedback through the capacitor is that the output is the "integration" of the input. For a square wave input this results in a "saw tooth" output.

2.



Measure:

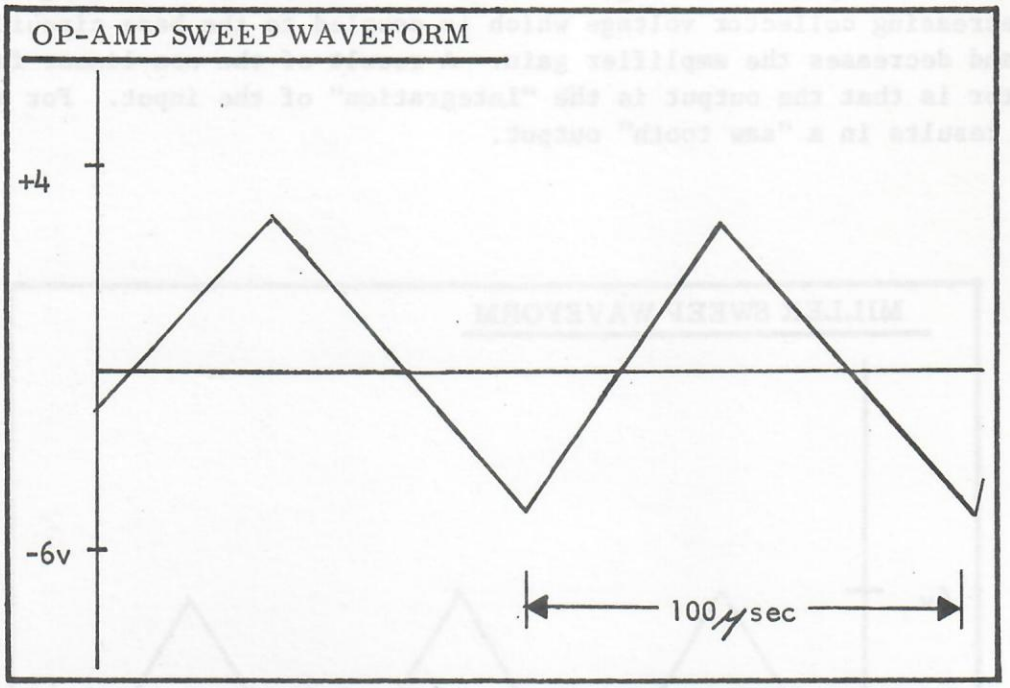
SWEEP AMPLITUDE	=	6 volts p-p
SWEEP TIME	=	50μsec

Calculate:

SWEEP RATE	=	10 KHz

MILLER SWEEP

4.



Measure

SWEEP VOLTAGE = 10 VOLTS

SWEEP TIME = 100 MICROSEC

Calculate

RATE $\frac{10 \text{ volts}}{50\mu\text{sec}}$ = 0.2 $\frac{\text{VOLTS}}{\text{MICROSEC}}$

5.

Calculate:

Rate = 0.212 $\frac{\text{VOLTS}}{\text{MICROSEC}}$

How does the measured rate compare with the theoretical rate?

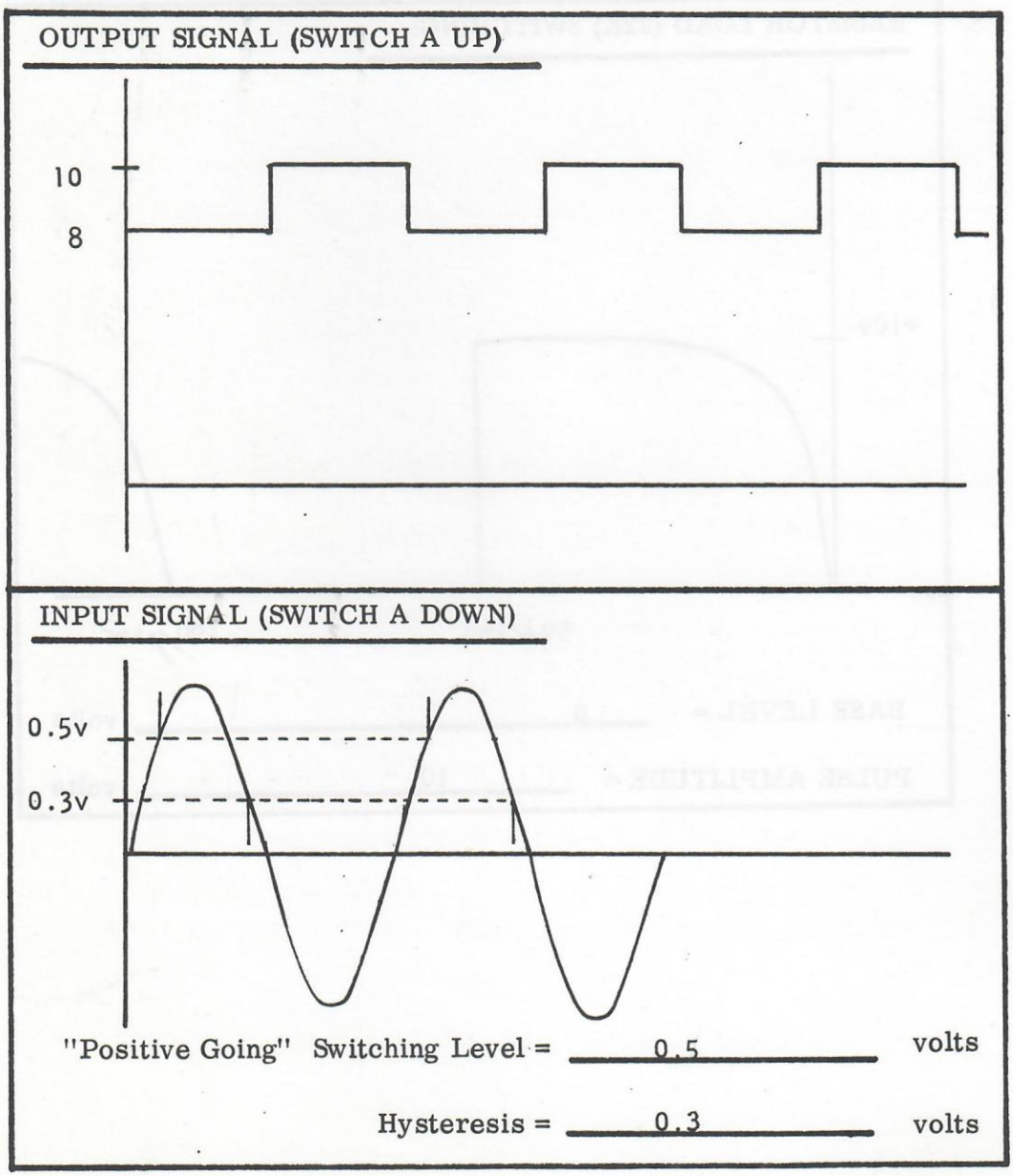
The Error is $E = \frac{0.212 - 0.2}{0.313} = \frac{0.012}{0.212} = 5\%$

This is very good experimental agreement.

SCHMITT TRIGGER

The Schmitt Trigger circuit is used where it is necessary to generate a sharp "switching" output from a noisy or slow speed signal. The main feature of the Schmitt Trigger is that the circuit turns ON at a predetermined threshold input voltage and then turns OFF at a lower voltage. This prevents the circuit from being driven in such a way that the input voltage is just at the ON/OFF voltage and the circuit turns ON and OFF erratically.

3.



"Positive Going" Switching Level = 0.5 volts

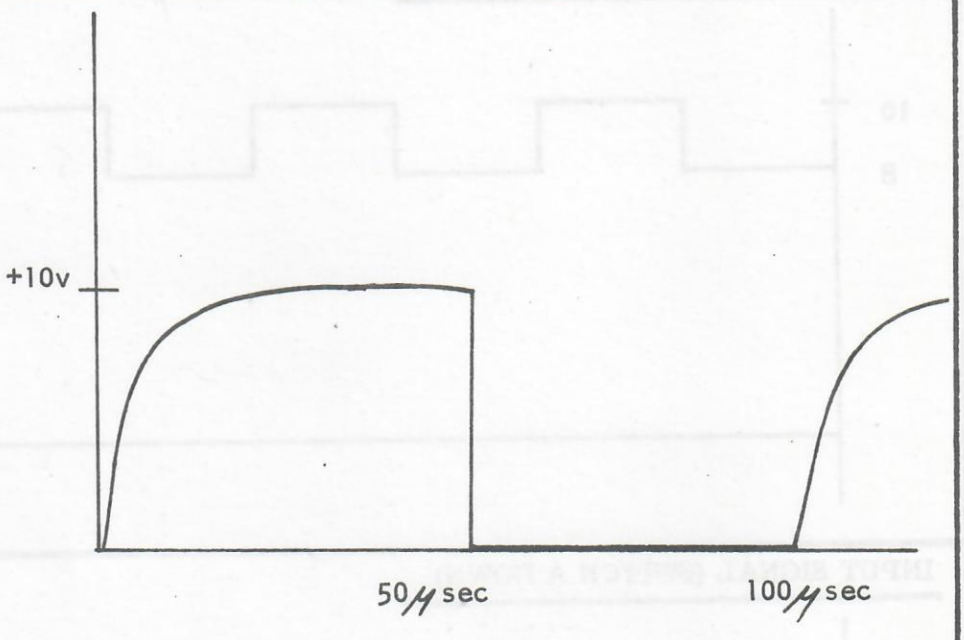
Hysteresis = 0.3 volts

INDUCTIVE DRIVER

The inductive voltage developed across an inductor in a switching circuit is studied. The reactance of the coil (stored energy) causes a very high voltage to be developed across the inductor. The magnitude of this voltage is measured and the theoretical value is calculated. This high voltage is generally not desirable in solid-state circuits. A technique of diode limiting is used to eliminate this voltage spike.

4.

RESISTOR LOAD (22K) SWITCHING:

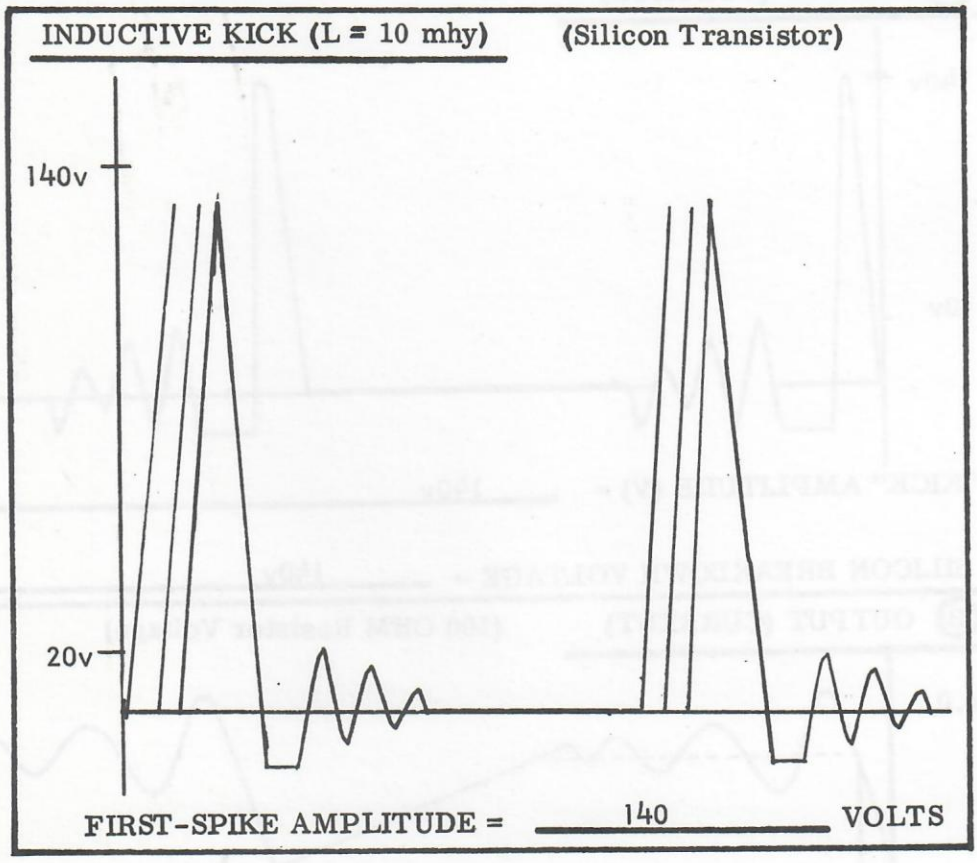


BASE LEVEL = 0 volts

PULSE AMPLITUDE = 10 volts

INDUCTIVE DRIVER

6.



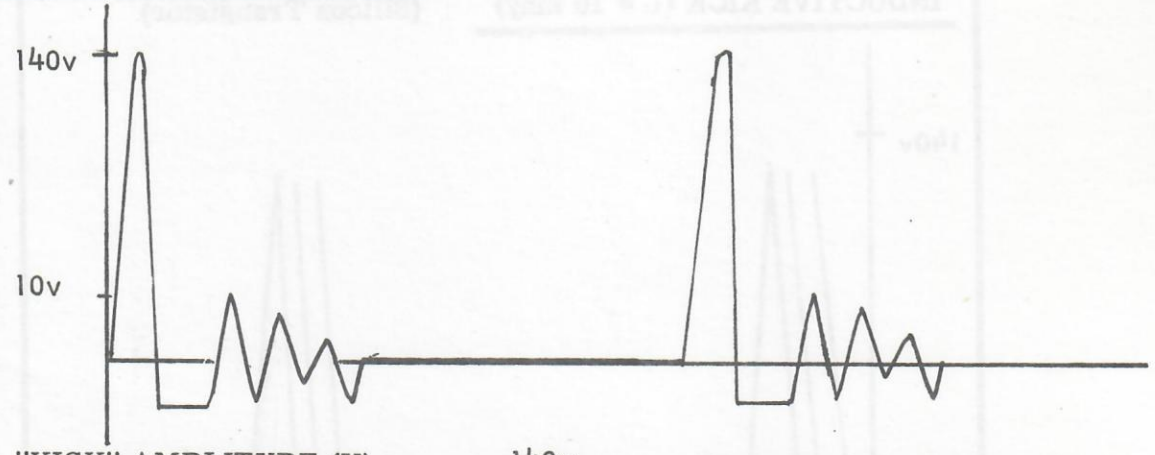
INDUCTIVE DRIVER

7.

INDUCTIVE KICK WAVESHAPES

(Reduce +V1 to PREVENT CLIPPING)

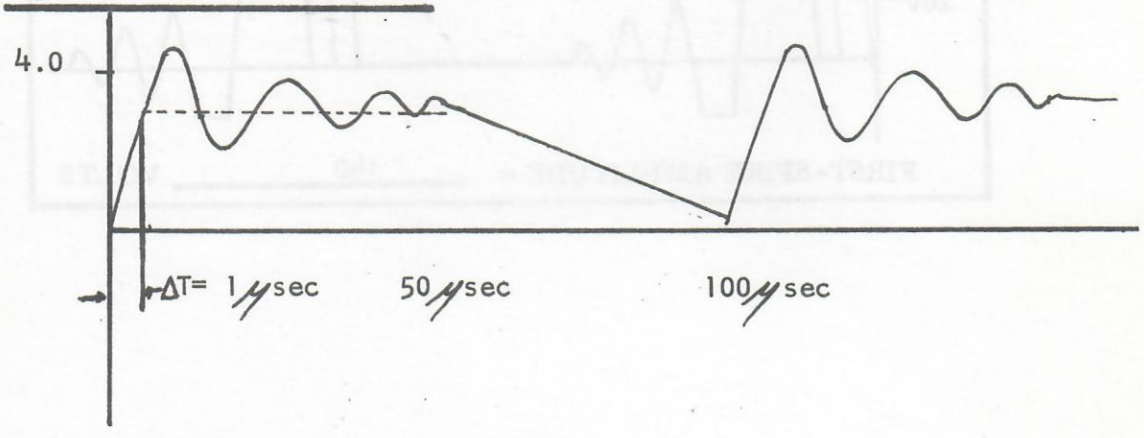
Ⓐ OUTPUT (VOLTAGE)



"KICK" AMPLITUDE (V) = 140v

SILICON BREAKDOWN VOLTAGE = 140v

Ⓑ OUTPUT (CURRENT) (100 OHM Resistor Voltage)



CURRENT-OFF (Rise-Time) (ΔT) = 1 microsecs.

PULSE AMPLITUDE (E) = 1.5 volts.

SUPPLY VOLTAGE (Use oscilloscope)

+V1 VOLTAGE = 4 volts.

INDUCTIVE DRIVER

8.

$$\Delta I = \frac{E}{100} = \frac{1.5}{100} = 15 \text{ ma}$$

$$\boxed{\Delta I = 15 \text{ ma}}$$

$$V_T = L \frac{\Delta I}{\Delta T} = 10 \times 10^{-3} \frac{15 \times 10^{-3}}{10^{-6}} = \frac{150 \times 10^{-6}}{2 \times 10^{-6}} = 150 \text{ volts}$$

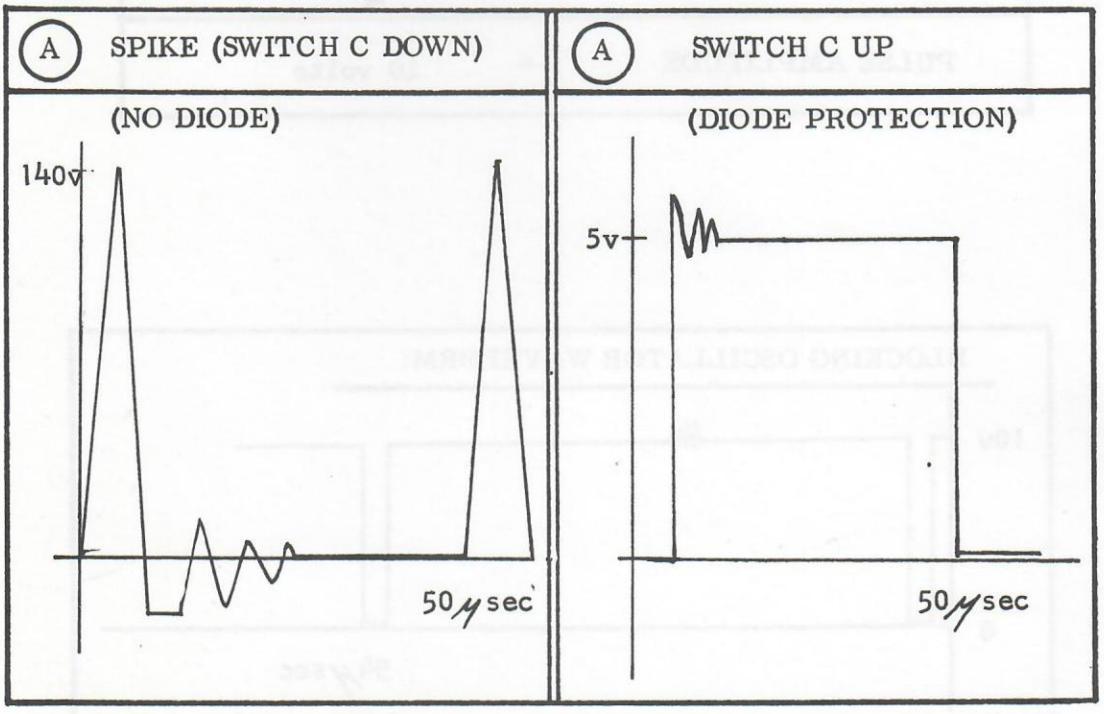
$$\boxed{V_T = 150 \text{ volts}}$$

How does the calculated (V_T) and the measured (V) compare?

The measured V_T is within 10% of the theoretical value of V_T of 150 volts.

10.

WAVEFORMS



BLOCKING OSCILLATOR

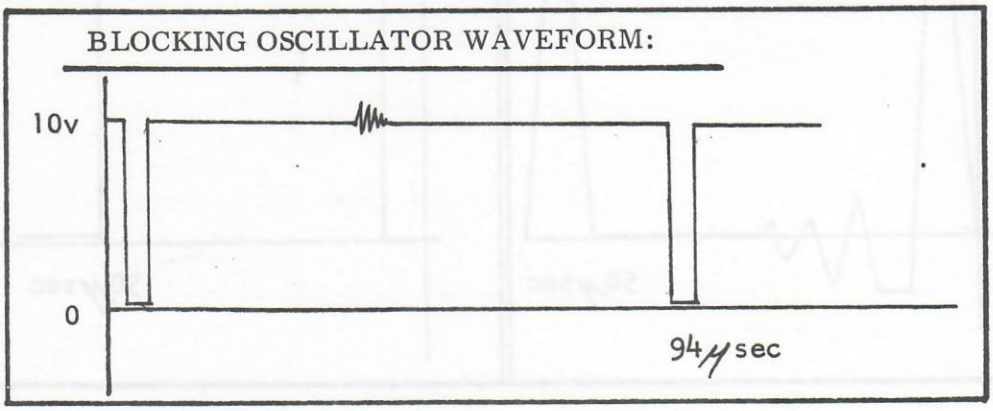
The blocking oscillator combines the features of the high frequency feedback oscillator with the principles of the relaxation oscillator. The phase relationship necessary for oscillation is provided by the transformer. The R.C. Time Constant of the base resistor and the base capacitor control the period of oscillation of the circuit.

When the transistor begins to saturate the transformer secondary dotted terminal will become positive, which will drive the transistor further into saturation. After the transistor is saturated the collector current will stabilize and the induced voltage at the secondary will decrease. The 0.01 μfd capacitor will discharge through the base-emitter junction of the transistor and the transistor will come out of saturation. This action results in a pulse oscillation.

4.

NEGATIVE PULSE WIDTH	=	1.5 μsec
PULSE PERIOD	=	94 μsec
PULSE AMPLITUDE	=	10 volts

BLOCKING OSCILLATOR WAVEFORM:



BLOCKING OSCILLATOR

5.

	MIN R POT	MAX R POT
PERIOD (μ sec)	25μ sec	150μ sec
PULSE WIDTH (μ sec)	2μ sec	1.5μ sec

Varying the circuit R effects both the pulse width and the period. The period is effected most dramatically.

6.

BASE-TUNED BLOCKING OSCILLATOR

Capacitance (set R = 10K	Pulse Period	Pulse Width
.01 mfd	150μsec	1.5μsec
.001 mfd	15μ sec	1.0μ sec
.25 mfd	2.7 msec	6.0μsec
1 mfd	11 msec	*2 pulses are present 110μsec apart 15μsec in duration

BLOCKING OSCILLATOR

8.

EMITTER-TUNED BLOCKING OSCILLATOR

CAPACITOR	.01 mfd	.25 mfd
PULSE WIDTH	1 μsec	4 μsec
MAXIMUM PERIOD	160 μsec	2.7 msec
MINIMUM PERIOD	12 μsec	100 μsec

DIODE LOGIC GATES: AND - OR

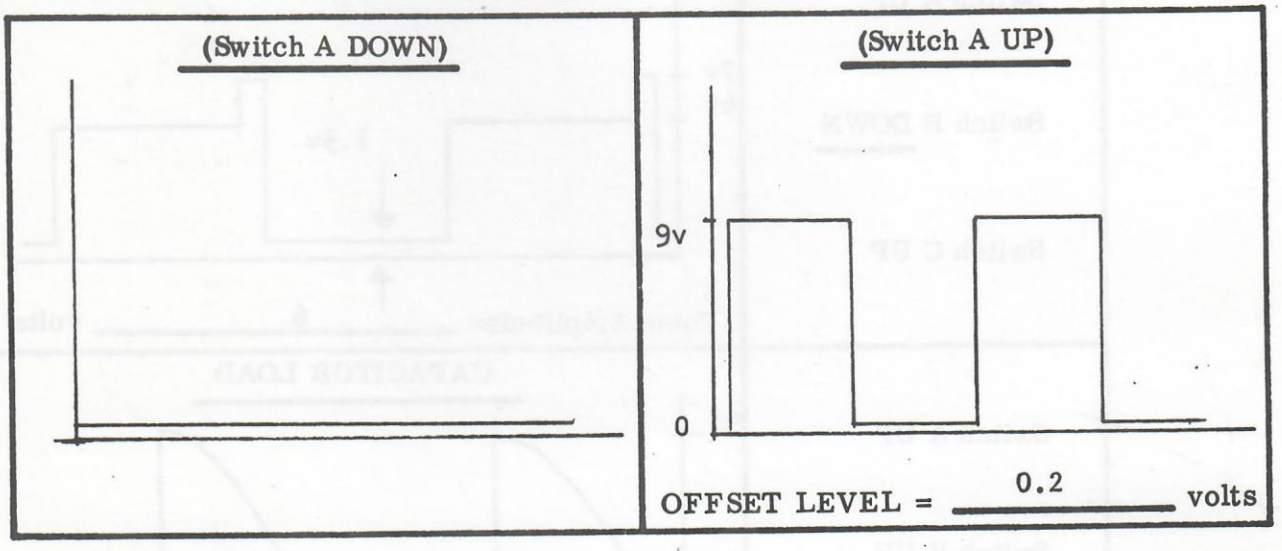
The Diode Logic AND and OR gates demonstrate the application of Diodes to control Binary or ON-OFF signals. The basic description of the circuit operation is covered in the experiment.

The effects of Resistive and Capacitive Loading on these circuits is also studied.

Note that the Diode AND gate has 2.2K resistance to +V1 when the output is "high" and has only 30 - 100 ohms resistance to ground of the forward biased diode when the output is "low". Therefore we would expect to see the resistive and capacitive loading effects primarily in the "high" state where the gate impedance is large. The reverse is true of the Diode OR gate because the dodes are reversed. These loading effects cause the diode logic gates to be generally unacceptable for use in logic circuits although they can be used for specific applications where there will be no loading.

2.

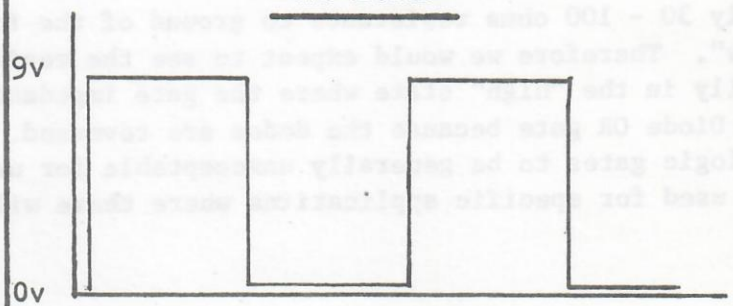
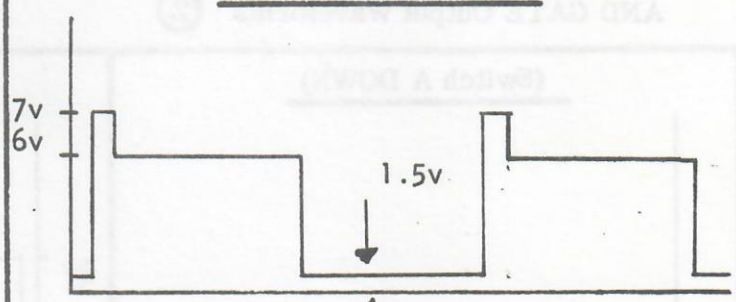
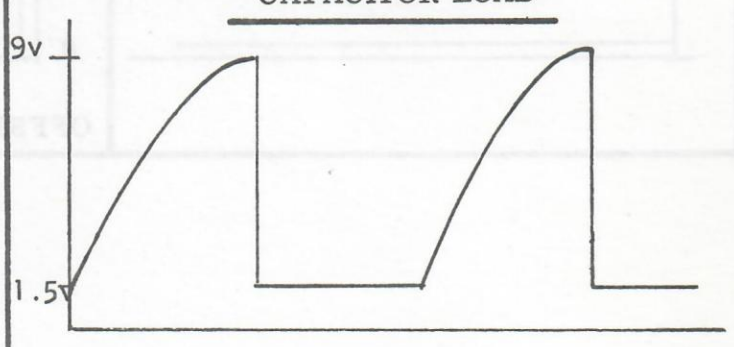
AND GATE Output Waveforms (Z)



DIODE LOGIC GATES: AND - OR

3.

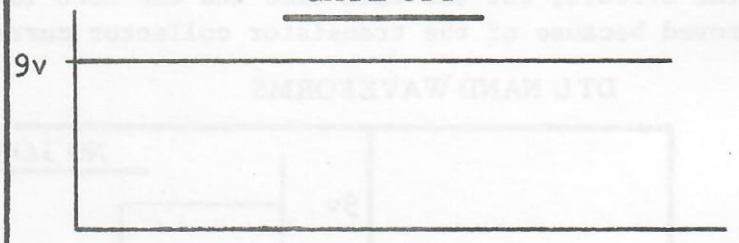
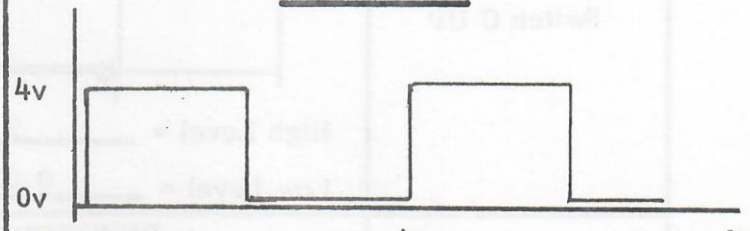
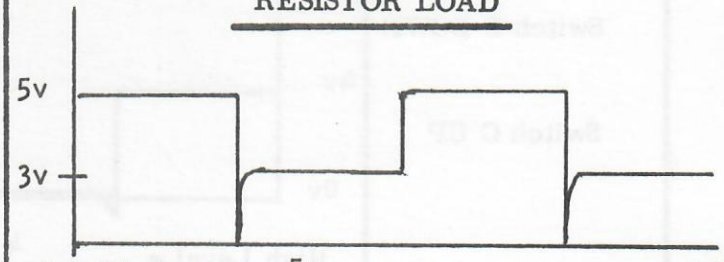
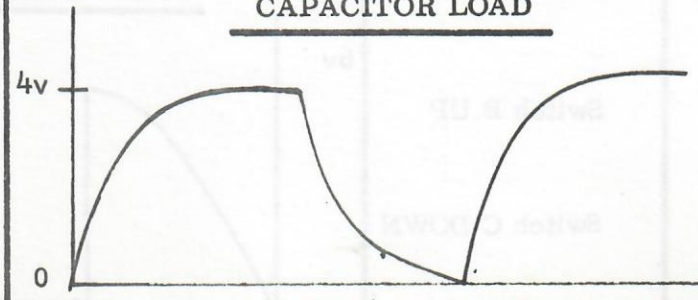
DIODE AND GATE Loading Waveforms

Switch A UP Switch B UP Switch C UP	NO LOAD  Pulse Amplitude = 9 volts
Switch A UP Switch B DOWN Switch C UP	RESISTOR LOAD  Pulse Amplitude= 6 volts
Switch A UP Switch B UP Switch C DOWN	CAPACITOR LOAD  Rise Time = 50 micro seconds

DIODE LOGIC GATES: AND - OR

4.

DIODE OR GATE Loading Waveforms

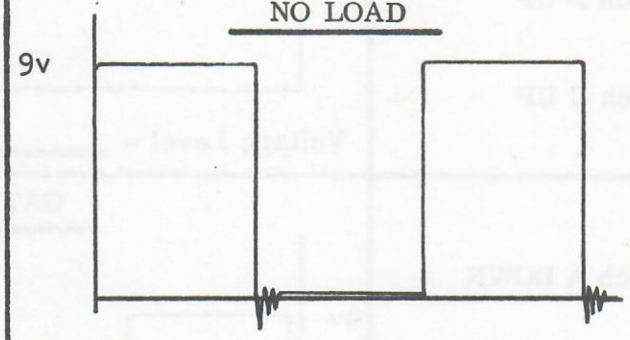
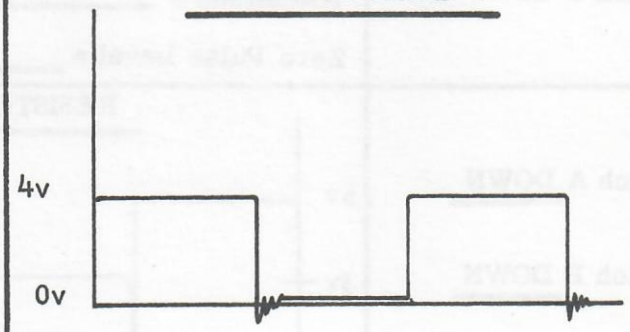
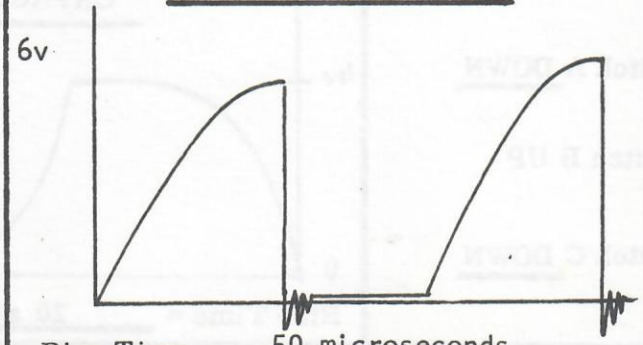
Switch A UP Switch B UP Switch C UP	GATE OFF  Voltage Level = 9 volts
Switch A DOWN Switch B UP Switch C UP	GATE ON  Amplitude = 4 volts Zero Pulse Level = 0 volts
Switch A DOWN Switch B DOWN Switch C UP	RESISTOR LOAD  Amplitude = 5v volts Zero Pulse Level = 3 volts
Switch A DOWN Switch B UP Switch C DOWN	CAPACITOR LOAD  Rise Time = 20 microseconds

DTL NAND

These circuits are examples of Diode Logic Gates followed by a transistor output drive stage which will prevent the extreme loading effects noted with the simple Diode Logic gates. Gates of this type are called Diode-Transistor Logic and are abbreviated as DTL gates.

Note that the transistor drive stage will not help the loading effects on the rise time of the circuit, but the fall time and the Zero level of the gate output will be much improved because of the transistor collector current sinking capability.

DTL NAND WAVEFORMS

Switch B UP Switch C UP	NO LOAD  High Level = 9 volts Low Level = 0.02 volts
Switch B DOWN Switch C UP	RESISTOR LOAD  High Level = 4 volts Low Level = 0.02v volts
Switch B UP Switch C DOWN	CAPACITOR LOAD  Rise Time = 50 microseconds Fall Time = 0.5 microseconds

DTL NAND

2.

TRUTH TABLE

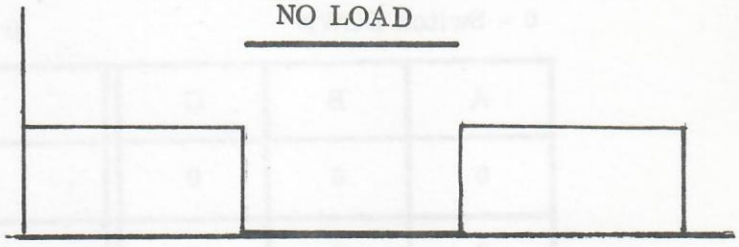
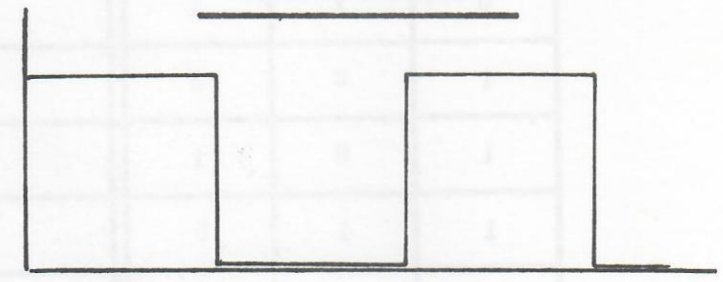
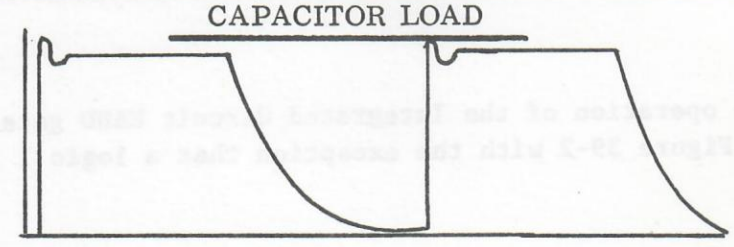
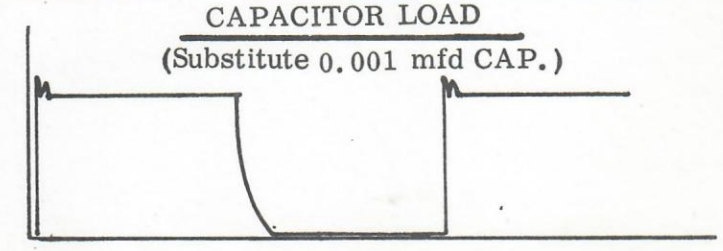
INPUTS			OUTPUT
1 = Switch UP			1 = High volts
0 = Switch DOWN			0 = Low volts
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

5. The operation of the Integrated Circuit NAND gate is the same as the DTL gate wired in Figure 39-2 with the exception that a logic 1 is 4.7 volts D.C.

EMITTER FOLLOWER DRIVER

The Emitter Follower or Common Collector Pulse Drive circuit is used. Note that this circuit has very low impedance drive to +V when the transistor is ON so the rise times are short and can drive capacitive loads. When the circuit output is zero, the transistor is OFF and the load must discharge to ground via the 1K emitter resistor. This will cause the fall time of the circuit to be effected by loading.

2. E.F. DRIVER WAVEFORMS

Switch A UP Switch B UP	NO LOAD  Pulse Amplitude = 9 volts Rise Time = Less than 0.5 μsec
Switch A DOWN Switch B UP	RESISTOR LOAD  Pulse Amplitude = 9v
Switch A UP Switch B DOWN	CAPACITOR LOAD  Rise Time = 2 microseconds Fall Time = 40 microseconds
Switch A UP Switch B DOWN	CAPACITOR LOAD (Substitute 0.001 mfd CAP.)  Rise Time = 0.25 microseconds Fall Time = 4 microseconds

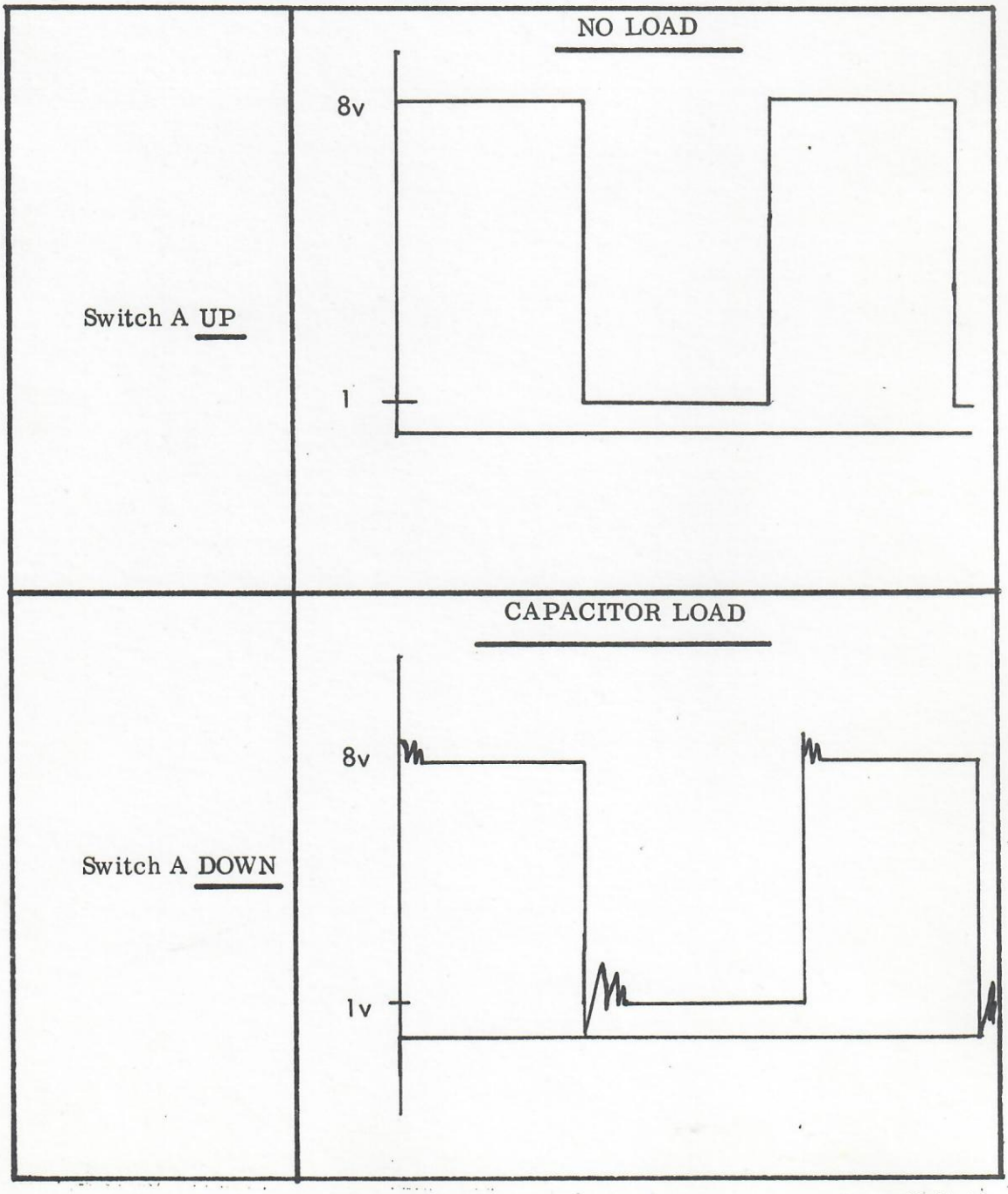
EMITTER FOLLOWER DRIVER

Note that the current drive capability of the transistor makes the output rise times short in spite of capacitive loading. The fall time, however, is dependent upon the 1K emitter resistor (the transistor is OFF) and this causes a significant fall time with capacitive loads.

COMPLEMENTARY EMITTER FOLLOWER

This type of circuit is used when an active pull up and an active pull down are required for an output with fast rise and fall times and the ability to drive capacitive loads. Transistor Q4 will provide low impedance charging to positive voltages and Q1 will provide a low impedance discharge path to ground. Note that the base of Q1 is driven to ground by the square wave input. The emitter of Q1 will, therefore, never attain a good, hard ground level, but will always float above ground by the offset of the emitter above the base voltage in transistor Q1.

2. COMPLEMENTARY E.F. DRIVER WAVEFORMS



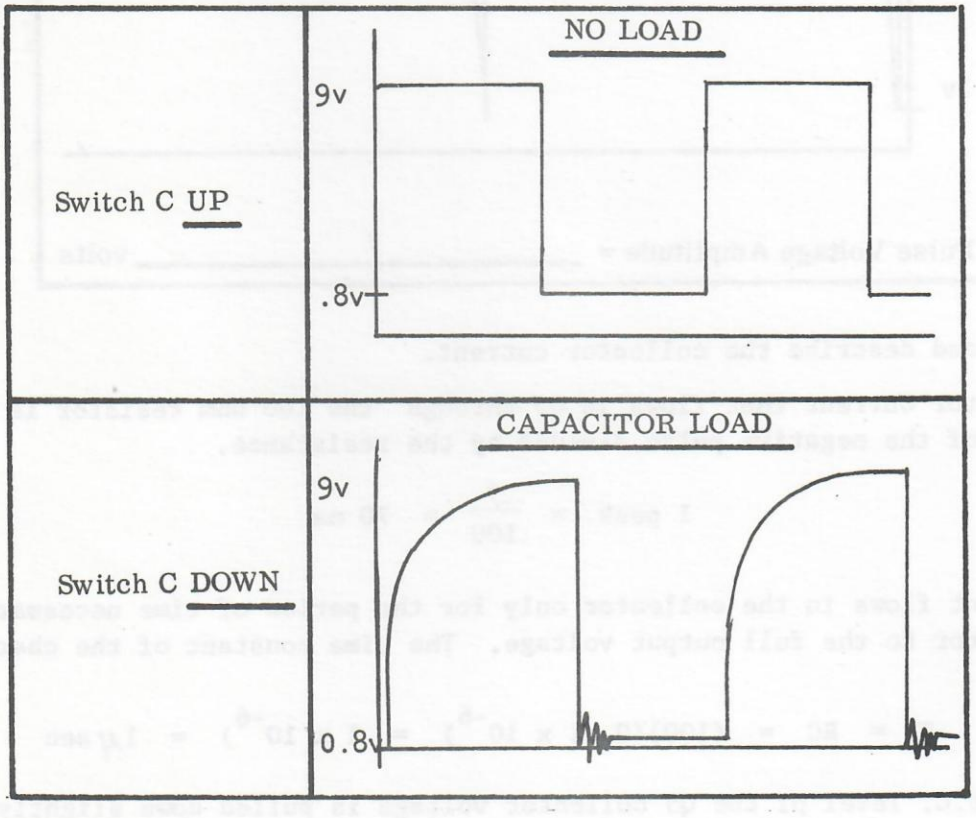
Note that the rise and fall times of the output waveforms are very fast.

TOTEM POLE DRIVER

The Totem Pole Driver uses only NPN transistors which make fabrication into a single Integrated Circuit module very simple from a production point of view. Note that each transistor has an extra diode in the emitter circuit. These diodes add an extra diode voltage drop or offset voltage to the base-emitter voltage required to turn each transistor ON. This assures that only one transistor will be ON at a time and the transistors will not both be competing with each other to drive the output circuit. The Output is driven to ground by a common emitter amplifier, so the Zero offset voltage will be the diode drop across D4.

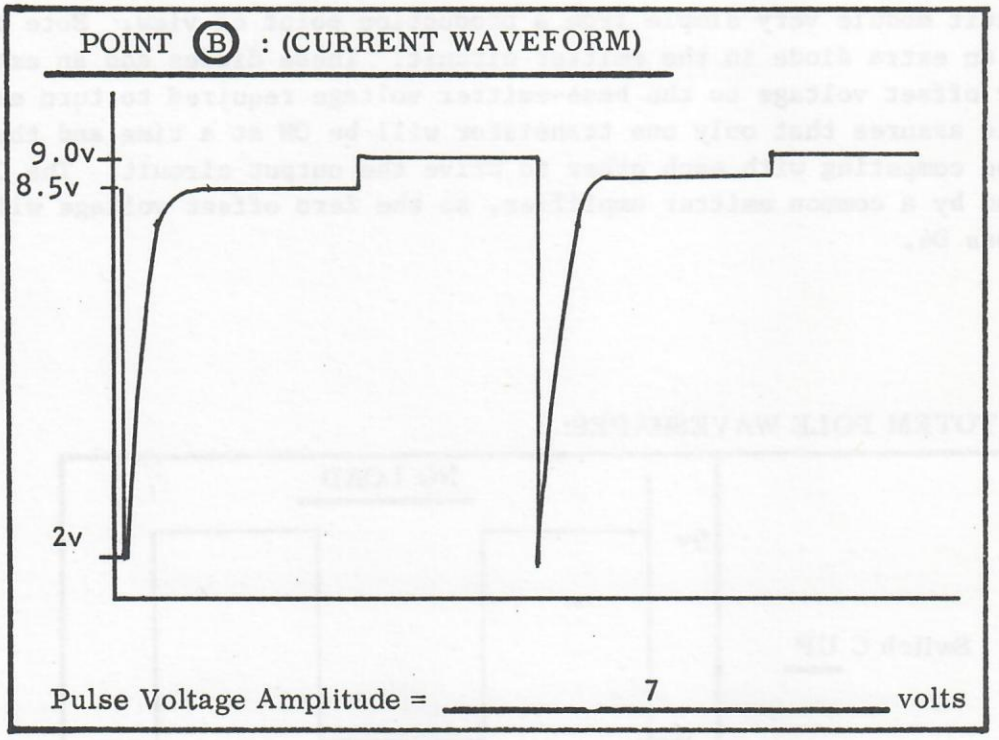
2.

TOTEM POLE WAVESHAPES:



TOTEM POLE DRIVER

3. TOTEM-POLE CURRENT WAVEFORM



4. Calculate and describe the collector current.

The Collector Current that flows in Q5 through the 100 ohm resistor is given by the magnitude of the negative pulse divided by the resistance.

$$I_{peak} = \frac{7}{100} = 70 \text{ ma}$$

This current flows in the collector only for the period of time necessary to charge the capacitor to the full output voltage. The time constant of the charging circuit is:

$$T = RC = (100)(0.01 \times 10^{-6}) = 1 \times 10^{-6}) = 1\mu\text{sec}$$

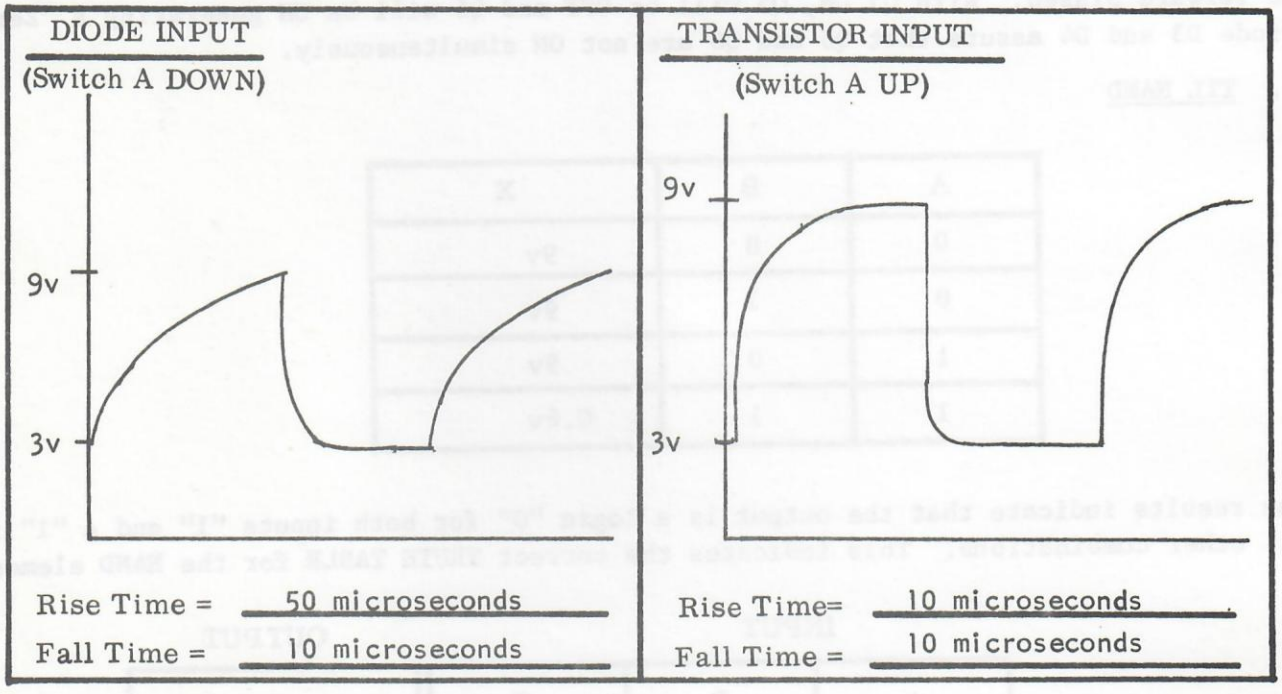
Note that the D.C. level of the Q5 collector voltage is pulled down slightly by the 3.3K resistive load when Q5 is ON. This represents the voltage output of the 100 ohm resistor in series with the 3.3K load.

COLLECTOR FOLLOWER

This circuit is typical of the input circuit provided on Transistor Transistor Logic (TTL) gates, where the transistor emitter is used as an input. When the input goes to Zero (Low) the transistor Collector Current pulls the Output and load to ground. Because of the small base resistor the transistor will be ON when the input is high. The base-emitter junction of the transistor is forward biased and the Signal Generator Pulse will provide current to charge the load, therefore, the Rise Time will be improved over the simple diode. This circuit, however, causes loading of the positive input pulse and requires drive current from the input signal. These drawbacks are eliminated in the next experiment which demonstrates the operation of a practical TTL gate.

1.

"AND" OUTPUT WAVEFORMS:



Note that the transistor circuit output is the same waveform as the Diode Circuit output WITH THE DIOE SHORT CIRCUITED. The purpose of the transistor emitter is to provide isolation of other inputs (other emitters) as seen in the next experiment.

TTL NAND CIRCUIT

The internal circuit of a TTL NAND gate is built using discrete components and the circuit is tested. In an Integrated Circuit Gate the emitter of Q4 would be especially manufactured to have several base emitter diodes to provide multiple inputs. This feature is simulated by using diodes D1 and D2.

When either input (A or B) is Ground (Zero) base current will flow in Q4. This base current will cause the Q4 collector to draw current FROM the base of Q7. Since this turns Q7 OFF the collector current in Q4 will consist of only the reverse base leakage current of Q7 and Q7 will be held firmly OFF. With Q7 off Q5 will be ON and Q6 will be OFF resulting in a High output.

When both inputs are "high" Q4 will be OFF and the base of Q7 will be driven ON via the 4.7K resistor in the base of Q4 and the base-collector diode junction of Q4, which will be forward biased. With Q7 ON, Q5 will be OFF and Q6 will be ON generating a "Zero" output Diode D3 and D4 assure that Q5 and Q6 are not ON simultaneously.

2. TTL NAND

A	B	X
0	0	9v
0	1	9v
1	0	9v
1	1	0.6v

The results indicate that the output is a logic "0" for both inputs "1" and a "1" for all other combinations. This indicates the correct TRUTH TABLE for the NAND element.

4.

1 = UP
0 = DOWN (Ground)

INPUT			OUTPUT
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

1 = ON (Hi volts)
0 = OFF (Lo volts)

Note that the 7400 NAND gates connected as shown in the figure yield the correct truth table.

RTL NOR & NAND

This family of Logic (RTL) is not used in modern logic systems. The circuits, however, do demonstrate the usage of transistors in logic systems and are an application of switching transistor theory.

2. TRUTH TABLE

A	B	C	NOR Fig. 45-1	NOR Fig. 45-2	NAND Fig. 45-3
0	0	0	1	1	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	0	1
1	0	0	0	0	1
1	0	1	0	0	1
1	1	0	0	0	0
1	1	1	0	0	0

4. Do both circuit outputs correspond to the NOR?

Yes both circuits are NOR circuits which have a "1" output when all inputs are "0".

8. Do the results correspond to the NAND function?

The output is "0" for both inputs "1". Therefore the circuit is a NAND gate.

RTL NOR & NAND

11. TRUTH TABLE

INPUTS		OUTPUT
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

12. By reveiwing the Truth Table, what logic "function" does this NOR Logic System perform?

This logic system is a NAND gate, when both inputs are "1" the output is "0".

ECL NOR

Emitter Coupled logic is used when very high switching speed is required. This type of logic belongs to the family of Non-saturated digital logic because the transistors are always in the active region. Because of this the transistor desaturation time is not lost during the switching cycle the logic is capable of higher speeds than saturated types of transistor logic.

2. Voltage Outputs

Binary Output	Voltage
High (1)	8.0 volts
Low(0)	5.5 volts

TRUTH TABLE

ECL NOR

INPUTS		OUTPUT
A	B	X
0	1	0
1	0	0
1	1	0
0	0	1

Note that the ECL gate LOW is not Ground. This is caused by the emitter resistor which makes the Q5 collector voltage positive when Q5 is ON.

HTL NAND

High Threshold logic requires a higher voltage input for a logic "1" than other logic gates. This requirement for a higher input voltage makes this type of gate "immune" to noise voltage at the input caused by sparking from motors or R.F. signals.

3. "1" and "0" Thresholds

INPUT B	VOLTAGE
"0"	0 to 2.5 volts
"1"	3.2 volts to 8.0 volts

Note that the input voltage must exceed 2.5 volts for any pulses to be noted at the gate output and must exceed 3.2 volts for a square wave to be transmitted by the gate. This represents a high threshold turn ON point.

C-MOS NOR

C-MOS logic is popular because of its high noise immunity, due to the high "1" level voltage and for its very low power supply drain which is a result of the low power consumption of FET circuitry. Another advantage of C-MOS is the very low input current required by each gate input because it is driving the gate of a FET. This also permits a larger"fan out" than practical in other logic families. "Fan out" is the number of gate inputs that can be driven by a single gate output.

The disadvantage of C-MOS is its relatively slow switching speed compared to TTL or ECL gates.

2. TRUTH TABLE

INPUT		OUTPUT
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

Do the results correspond to a NOR Gate? YES

3. I.C. 4001 TRUTH TABLE

INPUTS		OUTPUT
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

The system performs with NAND logic.

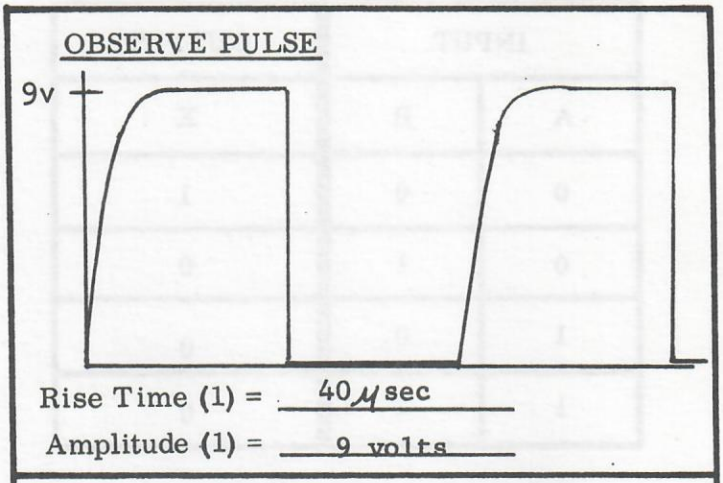
CAPACITIVE COMPENSATION ATTENUATOR

When a measurement is made with an oscilloscope the internal capacitance of the oscilloscope may load the signal and "round off" the waveform, giving a false impression of the actual signal waveform. In this experiment this effect is exaggerated by connecting 0.003 μfd cspacitance from the oscilloscope input to ground.

The method used to eliminate this capacitive loading effect is to use a compensated attenuator probe which has a parallel R.C. Network in series with the oscilloscope input and a shunt resistor to ground. The effect is to "tune out" the oscilloscope capacitance and eliminate the "rounding off" of the measured waveform.

2. OUTPUT WAVEFORMS

(1) SWITCH C DOWN

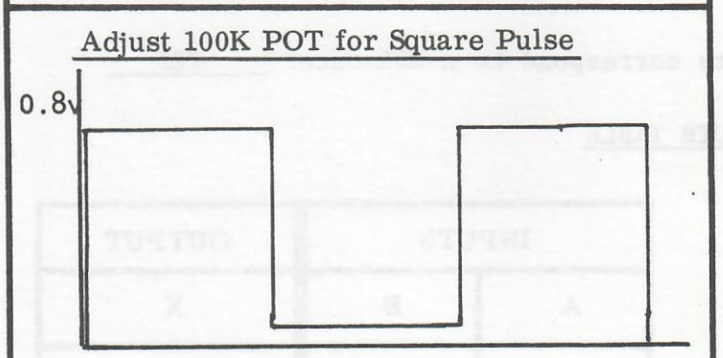


Rise Time (1) = 40 μsec

Amplitude (1) = 9 volts

(2) SWITCH C UP

(Compensation is in.)



Rise Time (2) = 2 μsec

Amplitude (2) = 0.8 volts

3. ATTENUATION

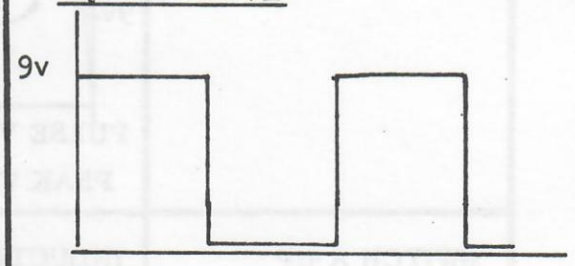
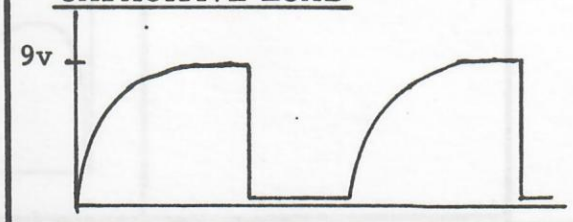
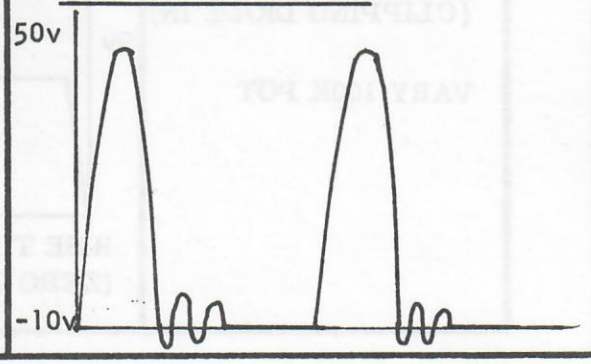
$$\text{ATTENUATION} = \frac{\text{AMPLITUDE (2)}}{\text{AMPLITUDE (1)}} = \frac{0.8}{9.0} = 0.089$$

ATTENUATION = 0.089

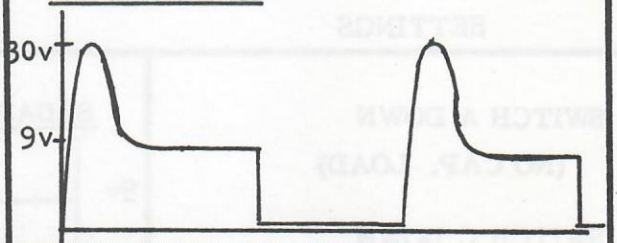
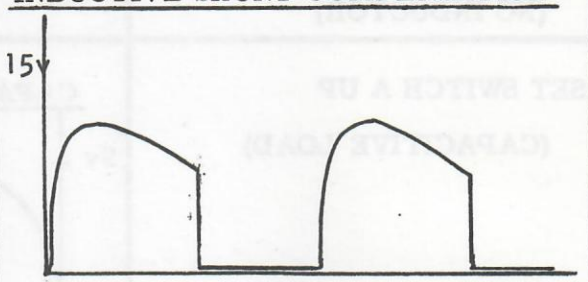
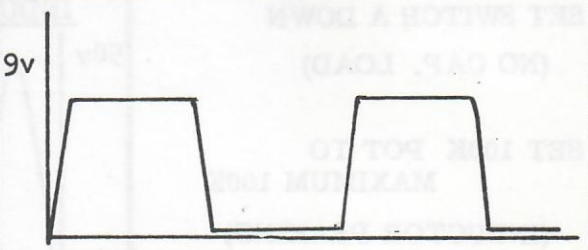
INDUCTIVE SHUNT COMPENSATION

This circuit uses an inductor in shunt with a capacitive load to eliminate the "rounding" of the measured waveform. This is an alternate method to capacitive compensation. The advantage of using this type of compensation network is that the circuit causes no attenauation of the waveform as found for the series compensator.

4.

SETTINGS	WAVEFORMS
SWITCH A DOWN (NO CAP. LOAD) SWITCH C DOWN (NO DIODE CLIP.) 100K POT. TO ZERO (NO INDUCTOR)	SQUARE WAVE 
SET SWITCH A UP (CAPACITIVE LOAD)	CAPACITIVE LOAD 
SET SWITCH A DOWN (NO CAP. LOAD) SET 100K POT TO MAXIMUM 100K (INDUCTOR PEAKING)	INDUCTOR PEAKING 

INDUCTIVE SHUNT COMPENSATION

SETTINGS	WAVE FORMS
ADJUST 100K POT FOR SINGLE PEAK	SINGLE PEAK  PULSE VOLTAGE LEVEL = 9v PEAK VOLTAGE LEVEL = 30v
SWITCH A UP (CAP. LOAD)	INDUCTIVE SHUNT COMPENSATION 
KEEP SWITCH A UP SWITCH C UP (CLIPPING DIODE IN) VARY 100K POT	PULSE CLIPPING  RISE TIME: (ZERO TO FULL LEVEL) = 10 μsec

DIGITAL TO ANALOG CONVERTER

The three resistors and the switch connections comprise a switched voltage divider network which generates a voltage output proportional to the binary code input. When all the switches are DOWN, binary number zero, the output voltage will be zero because all resistors are connected to ground. As the switches are manipulated the output voltage will vary proportionally to the binary number input. The output voltage can be calculated by using the parallel resistor formula and the Superposition Theorem 4.

1 = UP
0 = DOWN

DIGITAL SWITCHES			ANALOG	
A	B	C	NUMBER	READ VOLTAGE
4	2	1	—	—
0	0	0	0	0
0	0	1	1	1.0
0	1	0	2	1.9
0	1	1	3	2.9
1	0	0	4	3.9
1	0	1	5	4.9
1	1	0	6	6.0
1	1	1	7	7.0

DIGITAL INTEGRATED CIRCUITS

This experiment utilizes the Integrated Circuits to implement two digital systems. The intent is to familiarize the student with the Data Sheets and specifications of Digital Integrated Circuits and to provide practice in using I.C.'s.

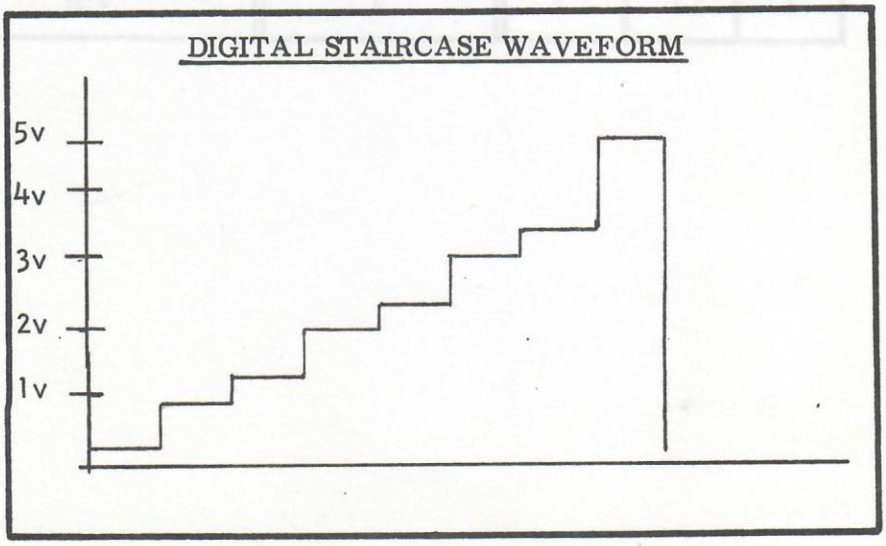
4.

	INPUT	OUTPUT "Q"
	A, B, C DOWN	1
	A UP	1
SET →	A UP, B UP	1
	A DOWN, B DOWN	1
	B UP	1
CLEAR →	B UP, C UP	0
	A DOWN, B DOWN, C DOWN	0
	B DOWN, A UP	0
SET →	B DOWN, A UP, C UP	1

5. Does the logic circuit operate as a Memory?

When C is UP and A and B are DOWN then placing A UP then DOWN will set the memory to a 1. Placing B UP then DOWN will clear the memory to a "0".

8.



DIGITAL INTEGRATED CIRCUITS

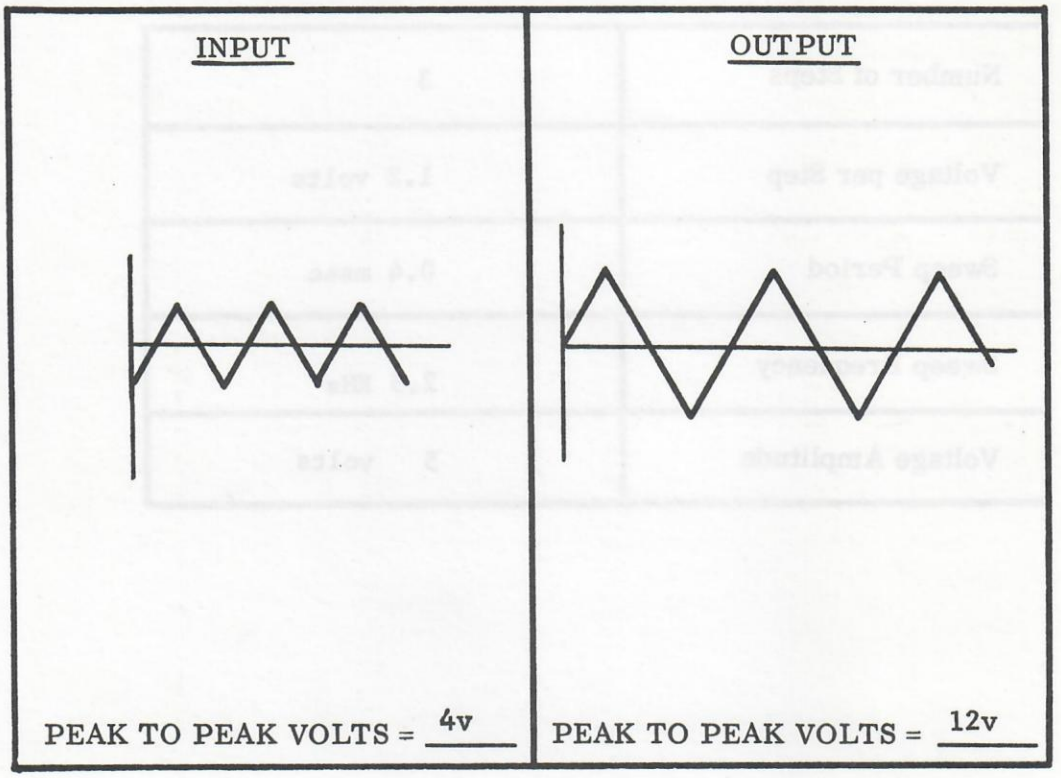
9.

Number of Steps	3
Voltage per Step	1.2 volts
Sweep Period	0.4 msec
Sweep Frequency	2.5 KHz
Voltage Amplitude	5 volts

LINEAR INTEGRATED CIRCUITS

This is a practical application of a Linear Integrated Circuit. The student will familiarize himself with the data sheets and specifications for linear I.C.'s and test the operation of a linear circuit.

3. WAVEFORMS



4.

$$\text{GAIN} = \frac{V_{output}}{V_{input}} = \frac{12}{4} = 3$$

GAIN = 3

5. How does the MEASURED GAIN compare with the designed gain of -3? What is the output voltage variation range? What is the input voltage variation range?

The Measured Gain and the design gain are the same. This circuit is a high precision circuit with very predictable gain, which is one reason that OP-AMP circuits are very popular and widely used.

The Output voltage variation range is 0 to 16 volts.

The Input voltage variation range is 0 to 5.3 volts.

LINEAR INTEGRATED CIRCUITS

6.

R_{IN}	R_F	CALCULATE GAIN	MEASURE GAIN
3.3K	10K	3 ,	3
3.3K	3.3K	1	1
3.3K	33K	10	10
3.3K	100K	30	29
3.3K	1K	0.3	0.30
3.3K	100K POT	0 to 30	0 to 30
10K	33K	3.3	3.3
10K	1M POT	0 to 100	0 to 100

7. Substitute the above resistors and measure the gain. How do the measured gains compare with the calculated gains?

The measured Gain for the circuits in step 6 are very close to the theoretical Gain. The actual accuracy of the Gain is dependent upon the accuracy of the resistors.

R_{IN}	R_F	CALCULATE GAIN	MEASURE GAIN
2.0K	10K		
2.0K	20K		
2.0K	30K		
2.0K	100K		
2.0K	1M		
2.0K	100K POT		
10K	30K		
10K	1M POT		

PULSE & WAVESHAPING BOOK V (formerly ELECTRONICS BOOK III or BOOK IV)

(FOR EDITION DATED, 1975, 1976, 1978, 1982)

UNIT 10

EXP. No. 2

page 1: Description line 1 change "Qt" to "Q5".

EXP. No. 3

page 1: Line 2 Change "You will set the TRANSISTOR "ON" and apply" to "A transistor which is biased "ON" will be momentarily turned OFF by applying."

page 2: Bottom line change "ΔT = 3 seconds" to "ΔT = 2.2 seconds."

EXP. No. 5

page 1: Change 1K resistor in the collector of Q5 to 3.3K.
Procedure step 2, change "with your finger" to "with TOUCH lead."
Remove 56K resistor to ground from "Touch" lead. Add 56K resistor to -V2 from the base of Q4.

EXP. No. 7

page 1: Schematic Diagram Figure 7-1 Add Test point (D) from base of Q2.

EXP. No. 8

page 1: Schematic Diagram Figure 8-1 Change both transistor base resistors from 3.3K to 10K.

page 5: Delete second sentence in Step 7.

EXP. No. 9

page 3: Schematic Diagram Figure 9-2 Change 3.3K resistor connected to the collector of Q5 to 2.2K.

EXP. No. 12

page 1: Schematic Diagram Figure 12-1 Change 220 pfd capacitor from Signal Generator Output to Anode of D1 to 0.01 mfd.

EXP. No. 14

page 5: Line 3 Change "5." to "6.".

EXP. No. 17

page 1: Schematic Diagram Figure 17-1 Change 100K resistor to ground to 10K.

page 2: Column marked RESISTANCE Change "100K" to "10K", Change "10K" to "4.7K".

EXP. No. 23

page 1: Schematic Diagram Figure 23-1 change 100 ohm resistor from 10K POT to ground to 2.2K.

UNIT 10

EXP. No. 24

page 1: Schematic Diagram Figure 24-1 add + to side of 10 mfd capacitor connected to the cathode of D1.

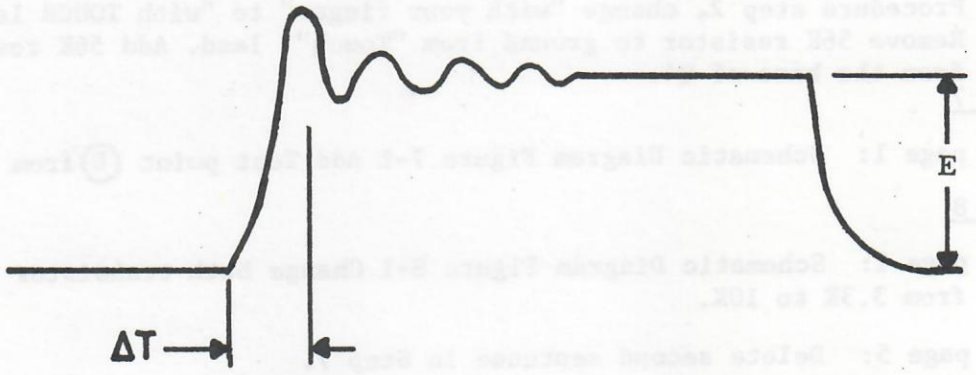
Description line 2 Change "changes" to "charges".

EXP. No. 36

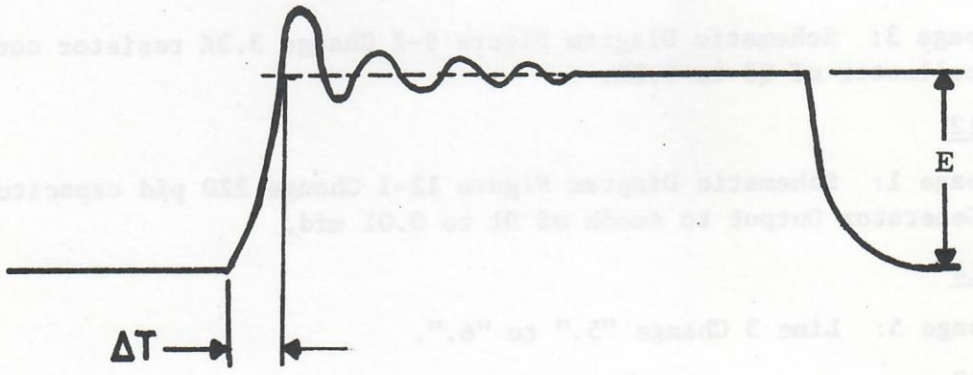
page 1: 3rd line from bottom change "patch" to "path".

page 5: Figure 36-2 (c)

Change from:



TO:



EXP. No. 38

page 3: CAPACITOR LOAD diagram

Change "Rise Time = _____ volts " to "Rise Time = _____ seconds".

EXP. No. 39

page 1: Schematic Diagram Figure 39-1 Change 10K resistor from base of Q7 to ground to 1K.

UNIT 10

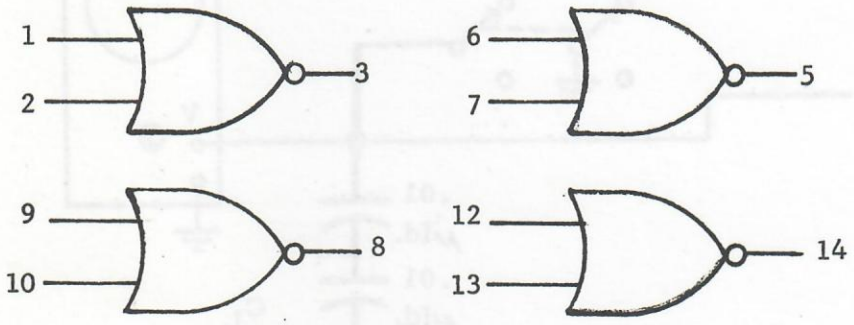
EXP. No. 43

page 1: Schematic Diagram Figure 43-1 Add "+V2" to +V Signal Generator Connection arrowhead.

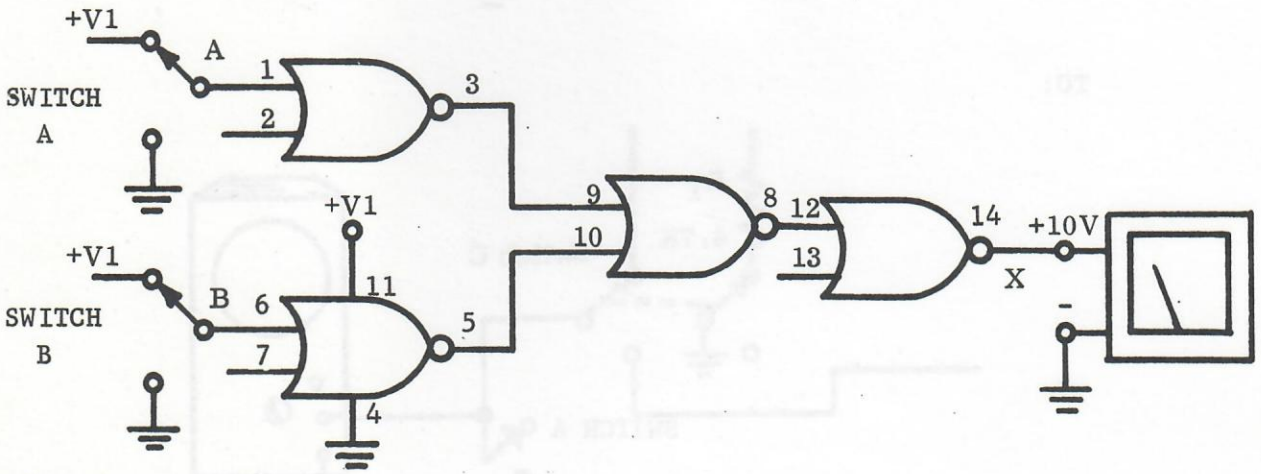
EXP. No. 45

page 4: Step 9 Change "718" to "717". Change "DUAL -3" to "QUAD -2". Change "Vcc 14" to "Vcc 11"

Change diagram Figure 45-4 to



page 5: Step 10 Change "718" to "717". Change Diagram Figure 45-5 the I.C. pin numbers to correspond to those shown in the diagram below.



EXP. No. 48

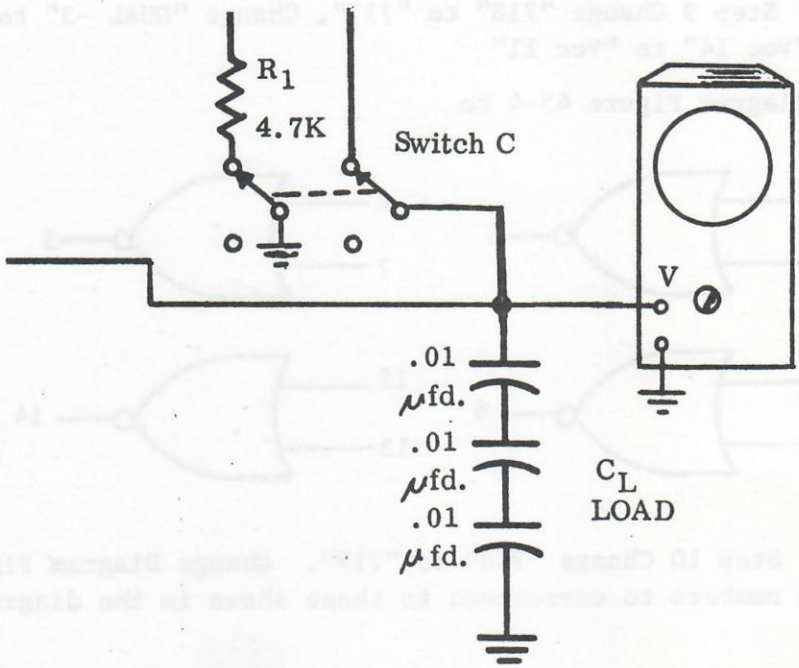
page 4: Diagram Figure 48-5 Add "SWITCH A" to switch connected to pin 1 Add "SWITCH B" to switch connected to pin 5 Add Notation "V_{DD} = Pin 14 = 10V" "V_{SS} = Pin 7 = GND."

UNIT 10

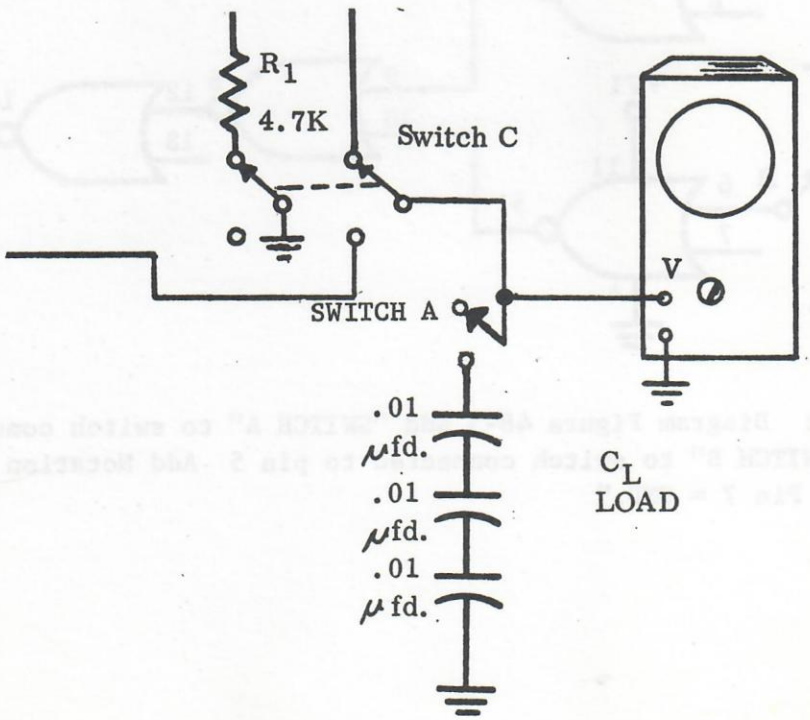
EXP. No. 49

page 1: Schematic Diagram Figure 49-1

Change FROM:



TO:



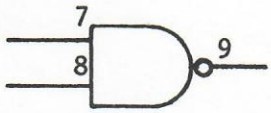
UNIT 10

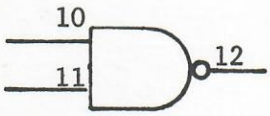
EXP. No. 52

page 1: Schematic Diagram Figure 52-1

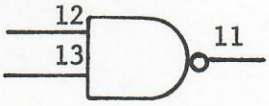
Change

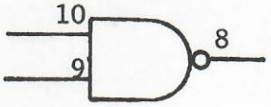
FROM:





TO:





Change "Connect +V1 ⟶ Pin 3" to "Connect +V1 ⟶ Pin 14"